NEC

MOS INTEGRATED CIRCUIT

μPD75104, 75106, 75108

4-BIT SINGLE-CHIP MICROCOMPUTER

DESCRIPTION

μPD75108 is a 4-bit single-chip microcomputer integrating timer/event counters, serial interface, and vector interrupt function, in addition to a CPU, ROM, RAM, and I/O ports, on a single chip. Operating at high speeds, the microcomputer allows data to be manipulated in units of 1, 4, or 8 bits. In addition, various bit manipulation instructions are provided to reinforce I/O manipulation capability. Equipped with I/Os for interfacing with peripheral circuits operating on a different supply voltage, outputs that can directly drive LEDs, and analog inputs, μPD75108 is suitable for controlling such systems as VTRs, acoustic products, button telephones, radio communications equipment, and printers. A pin-compatible EPROM model is also available for evaluation of system development and small-scale production of application systems.

Detailed functions are described in the following user's manual. Be sure to read it for designing.
μPD751XX Series User's Manual: IEM-922

FEATURES

- Internal memory
  - Program memory (ROM)
    : 8068 × 8 bits (μPD75108)
    : 6016 × 8 bits (μPD75106)
    : 4096 × 8 bits (μPD75104)
  - Data memory (RAM)
    : 512 × 4 bits (μPD75108)
    : 320 × 4 bits (μPD75106, 75104)
- New architecture "75X series" rivaling 8-bit microcomputers
- 43 systematically organized instructions
  - A wealth of bit manipulation instructions
  - 8-bit data transfer, compare, operation, increment, and decrement instructions
  - 1-byte relative branch instructions
  - GETI instruction executing 2-/3-byte instruction with one byte
- High speed. Minimum instruction execution time: 0.95 μs (at 4.19 MHz), 5 V
- Power-saving, instruction time change function: 0.95 μs/1.91 μs/15.3 μs (at 4.19 MHz)
- I/O port pins as many as 58
- Three channels of 8-bit timers
- 8-bit serial interface
- Multiplexed vector interrupt function
- Model with PROM is available: μPD75P108B (One-time PROM, EPROM)

Unless there are differences among μPD75104, 75106, and 75108 functions, μPD75108 is treated as the representative model throughout this manual.

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Date Published January 1994 P
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The mark ★ shows major revised points.

ORDERING INFORMATION

Part Number	Package	Quality Grade
μPD75104CW-xxx	64-pin plastic shrink DIP (750 mil)	Standard
μPD75104GF-xxx-3BE	64-pin plastic QFP (14 × 20 mm)	Standard
μPD75106CW-xxx	64-pin plastic shrink DIP (750 mil)	Standard
μPD75106GF-xxx-3BE	64-pin plastic QFP (14 × 20 mm)	Standard
μPD75108CW-xxx	64-pin plastic shrink DIP (750 mil)	Standard
μPD75108GF-xxx-3BE	64-pin plastic QFP (14 × 20 mm)	Standard

Remarks: xxx is ROM code number.

Please refer to "Quality Grade on NEC Semiconductor Devices" (Document Number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

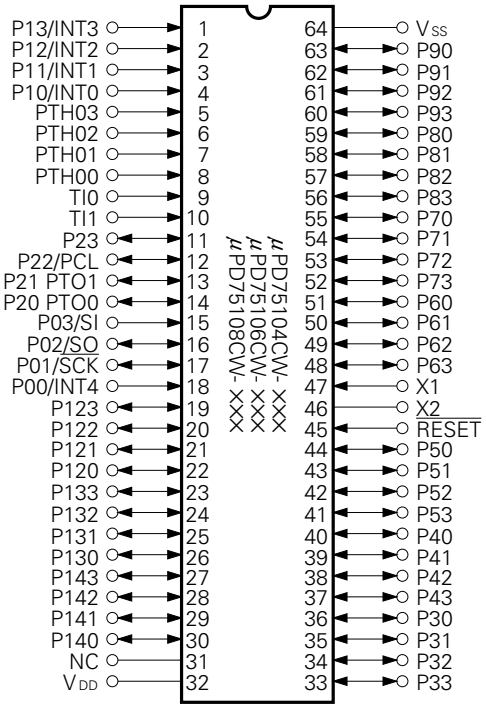
FUNCTIONAL OUTLINE

Item		Specifications
Number of Basic Instructions		43
Minimum Instruction Execution Time		Changeable in three steps: 0.95 μs, 1.91 μs, and 15.3 μs at 4.19 MHz
Internal Memory	ROM	8064 × 8 bits (μPD75108), 6016 × 8 bits (μPD75106), 4096 × 8 bits (μPD75104)
	RAM	512 × 4 bits (μPD75108), 320 × 4 bits (μPD75106, 75104)
General-Purpose Register		4 bits × 8 × 4 banks (memory mapped)
Accumulator		Three accumulators selectable according to the bit length of manipulated data: • 1-bit accumulator (CY), 4-bit accumulator (A), and 8-bit accumulator (XA)
I/O Port		58 port pins • CMOS input pins: 10 • CMOS I/O pins (can directly drive LEDs): 32 • Medium voltage N-ch open-drain I/O pins: 12 (can directly drive LEDs. Pull-up resistor can be connected to each bit) • Comparator input pins (4-bit accuracy): 4
Timer/Counter		• 8-bit timer/event counter × 2 • 8-bit basic interval timer (can be used as watchdog timer)
Serial Interface		• 8 bits • LSB first/MSB first mode selectable • Two transfer modes (transfer/reception and reception only modes)
Vector Interrupt		External: 3, Internal: 4
Test Input		External: 2
Standby		• STOP and HALT modes
Instruction Set		• Various bit manipulation instructions (set, reset, test, Boolean operation) • 8-bit data transfer, compare, operation, increment, and decrement • 1-byte relative branch instructions • GETI instruction constituting 2 or 3-byte instruction with 1 byte
Others		• Power-ON reset circuit (mask option) • Bit manipulation memory (bit sequential buffer: 16 bits)
Package		• 64-pin plastic shrink DIP (750 mil) • 64-pin plastic QFP (14 × 20 mm)

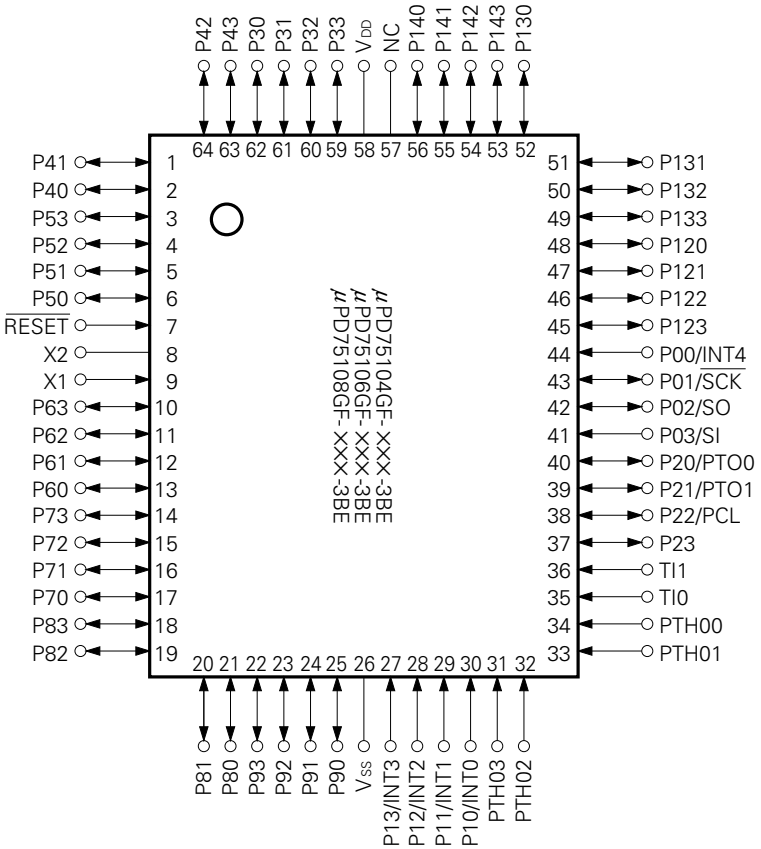
CONTENTS

1. PIN CONFIGURATION (Top View)

• 64-Pin Plastic Shrink DIP (750 mil)



• 64-Pin Plastic QFP (14 × 20 mm)

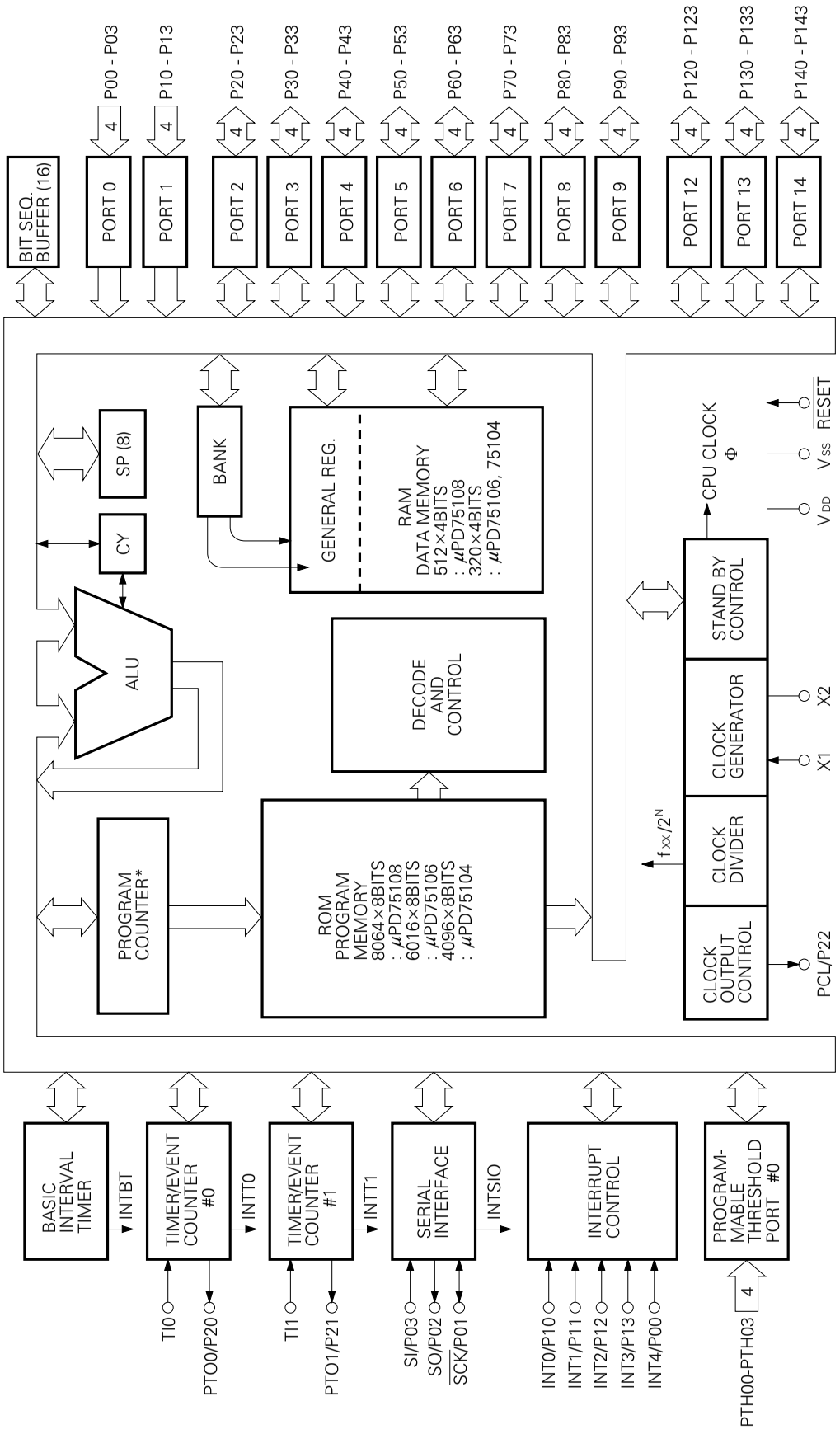


Pin names

P00-P03	: Port 0
P10-P13	: Port 1
P20-P23	: Port 2
P30-P33	: Port 3
P40-P43	: Port 4
P50-P53	: Port 5
P60-P63	: Port 6
P70-P73	: Port 7
P80-P83	: Port 8
P90-P93	: Port 9
P120-P123	: Port 12
P130-P133	: Port 13
P140-P143	: Port 14

$\overline{SCK}$	: Serial Clock Input/Output
SO	: Serial Output
SI	: Serial Input
PTO0, PTO1	: Timer Output
PCL	: Clock Output
PTH00-PTH03	: Comparator Input
INT0, INT1, INT4	: External Vector Interrupt Input
INT2, INT3	: External Test Input
TI0, TI1	: Timer Input
X1, X2	: Clock Oscillation Pin
$\overline{RESET}$	: Reset Input
NC	: No Connection

2. BLOCK DIAGRAM



*: 13 bits: μPD75106, 75108
12 bits: μPD75104

3. PIN FUNCTIONS

3.1 PORT PINS

Pin Name	I/O	Shared with:	Function	8-Bit I/O	At Reset	I/O Circuit TYPE*1
P00	Input	INT4	4-bit input port (PORT 0)	x	Input	B
P01	I/O	$\overline{SCK}$				F
P02	I/O	SO				E
P03	Input	SI				B
P10	Input	INT0	4-bit input port (PORT 1)		Input	B
P11		INT1				
P12		INT2				
P13		INT3				
P20*3	I/O	PTO0	4-bit I/O port (PORT 2)	x	Input	E
P21*3		PTO1				
P22*3		PCL				
P23*3		—				
P30-P33*3	I/O	—	4-bit programmable I/O port (PORT 3) Can be specified for input or output bitwise.		Input	E
P40-P43*3	I/O	—	4-bit I/O port (PORT 4)	o	Input	E
P50-P53*3	I/O	—	4-bit I/O port (PORT 5)		Input	E
P60-P63*3	I/O	—	4-bit programmable I/O port (PORT 6) Can be specified for input or output bitwise.	o	Input	E
P70-P73*3	I/O		4-bit I/O port (PORT 7)		Input	E
P80-P83*3	I/O	—	4-bit I/O port (PORT 8)	o	Input	E
P90-P93*3	I/O	—	4-bit I/O port (PORT 9)		Input	E
P120-P123*3	I/O	—	4-bit N-ch open-drain I/O port (PORT 12) Built-in pull-up resistors can be specified in bit units by mask option. Open-drain withstanding voltage: 12 V	o	Input*2	M
P130-P133*3	I/O	—	4-bit N-ch open-drain I/O port (PORT 13) Built-in pull-up resistors can be specified in bit units by mask option. Open-drain withstanding voltage: 12 V		Input*2	M
P140-P143*3	I/O	—	4-bit N-ch open-drain I/O port (PORT 14) Built-in pull-up resistors can be specified in bit units by mask option. Open-drain withstanding voltage: 12 V	–	Input*2	M

*1: Circles indicate Schmitt trigger input pins.
2: With drain open: high impedance
With pull-up resistor connected: high level
3: Can directly drive LEDs.

3.2 PINS OTHER THAN PORTS

Pin Name	I/O	Shared with:	Function	At Reset	I/O Circuit TYPE*1
PTH00-PTH03	Input	—	4-bit variable threshold voltage analog input port	—	N
TI0 TI1	Input	—	External event pulse inputs for timer/event counter. Also serves as edge-detected vector interrupt input. 1-bit input also possible.	—	B
PTO0	I/O	P20	Outputs for timer/event counter	Input	E
PTO1		P21			
$\overline{SCK}$	I/O	P01	Serial clock I/O	Input	F
SO	I/O	P02	Serial data output	Input	E
SI	Input	P03	Serial data input	Input	B
INT4	Input	P00	Edge-detected vectored interrupt input (both rising and falling edges detected)	Input	B
INT0	Input	P10	Edge-detected vectored interrupt inputs (valid edge selectable)	Input	B
INT1		P11			
INT2	Input	P12	Edge-detected testable inputs (rising edge detected)	Input	B
INT3		P13			
PCL	I/O	P22	Clock output	Input	E
X1, X2	—	—	Crystal/ceramic system clock oscillator connections. Input external clock to X1, and signal in reverse phase with X1 to X2.	—	—
$\overline{RESET}$	Input	—	System reset input (low level active type)	—	B
NC*2	—	—	No Connection	—	—
V_{DD}	—	—	Positive power supply	—	—
V_{SS}	—	—	GND	—	—

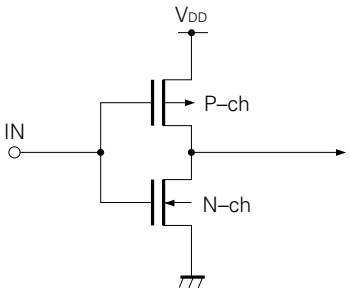
*1: Circles indicate Schmitt trigger input pins.

2: Connect the NC pin directly to the V_{DD} pin when μPD75P108B and a printed circuit board are shared.

3.3 PIN INPUT/OUTPUT CIRCUITS

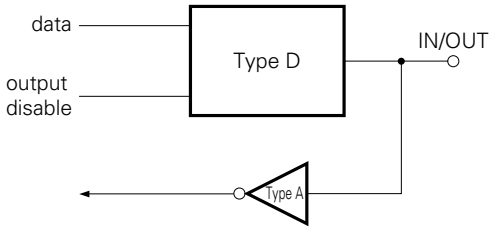
The following shows a simplified input/output circuit diagram for each pin of the μPD75108.

TYPE A



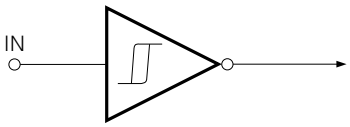
Input buffer of CMOS standard

TYPE E



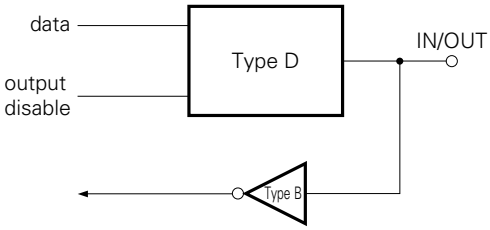
I/O circuit consisting of Type D push-pull output circuit and Type A input buffer

TYPE B



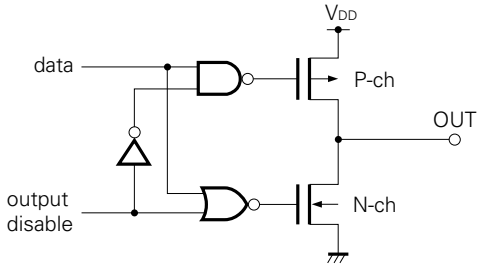
Schmitt trigger input with hysteresis characteristics

TYPE F



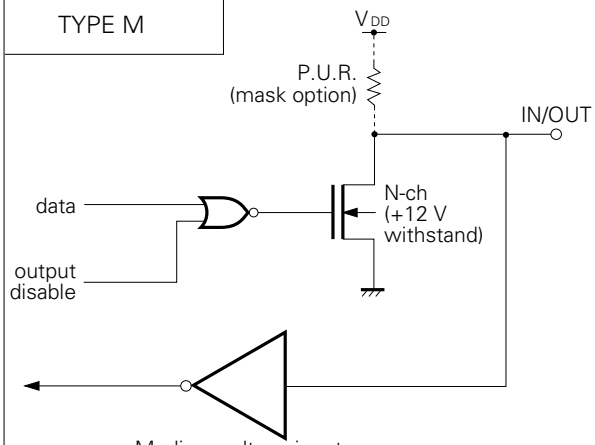
I/O circuit consisting of Type D push-pull output and Type B Schmitt trigger input

TYPE D

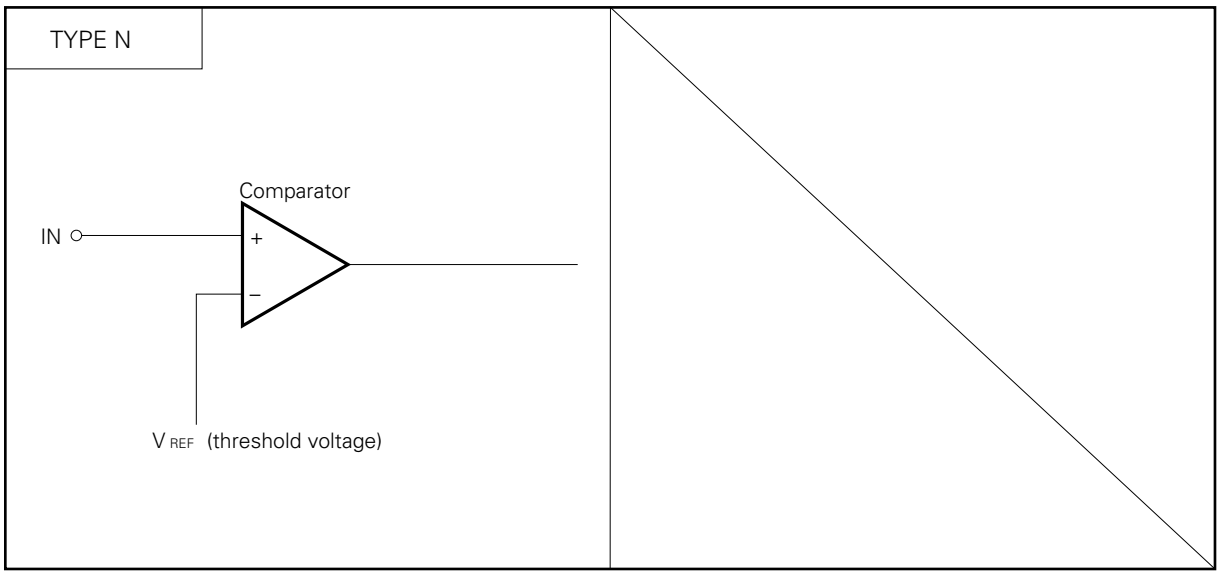


Push – pull output that can be set in a output high– impedance state (both P–ch and N–ch are off)

TYPE M



Medium-voltage input buffer (+12 V withstand)
P.U.R.: Pull-Up Resistor



3.4 RECOMMENDED PROCESSING OF UNUSED PINS

Pin	Recommended connections
PTH00-PTH03 TI0 TI1	Connect to V_{SS} or V_{DD}
P00	Connect to V_{SS}
P01-P03	Connect to V_{SS} or V_{DD}
P10-P13	Connect to V_{SS}
P20-P23 P30-P33 P40-P43 P50-P53 P60-P63 P70-P73 P80-P83 P90-P93 P120-P123 P130-P133 P140-P143	Input: Connect to V_{SS} or V_{DD} Output: Open
$\overline{\text{RESET}}$*1	Connect to V_{DD}
NC*2	Open

*1: Connect this pin to the V_{DD} pin only when a power-ON reset circuit is provided as a mask option.

2: Connect the NC pin to the V_{DD} pin when μPD75P108 and a printed circuit board are shared.

3.5 NOTES ON USING THE P00/INT4, AND $\overline{\text{RESET}}$ PINS

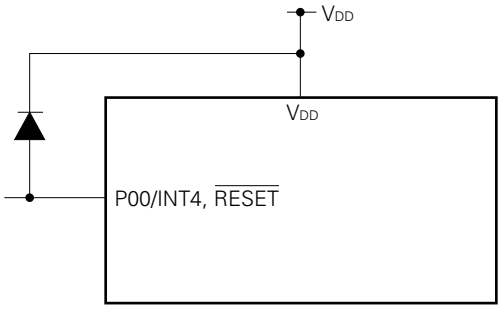
In addition to the functions described in Sections 3.1 and 3.2, an exclusive function for setting the test mode, in which the internal fuctions of the μPD75108 are tested (solely used for IC tests), is provided to the P00/INT4 and $\overline{\text{RESET}}$ pins.

If a voltage exceeding V_{DD} is applied to either of these pins, the μPD75108 is put into test mode. Therefore, even when the μPD75108 is in normal operation, if noise exceeding the V_{DD} is input into any of these pins, the μPD75108 will enter the test mode, and this will cause problems for normal operation.

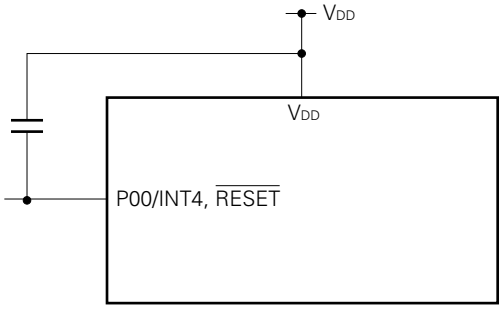
As an example, if the wiring to the P00/INT4 pin or the $\overline{\text{RESET}}$ pin is long, stray noise may be picked up and the above montioned problem may occur.

Therefore, all wiring to these pins must be made short enough to not pick up stray noise. If noise cannot be avoided, suppress the noise using a capacitor or diode as shown in the figure below.

- Connect a diode across P00/INT4 and $\overline{\text{RESET}}$, and V_{DD}.



- Connect a capacitor across P00/INT4 and $\overline{\text{RESET}}$, and V_{DD}.



4. MEMORY CONFIGURATION

- Program memory (ROM) ... 8064 × 8 bits (0000H-1F7FH) : μPD75108
  ... 6016 × 8 bits (0000H-177FH) : μPD75106
  ... 4096 × 8 bits (0000H-0FFFH) : μPD75104
  - 0000H, 0001H : Vector table to which address from which program is started is written after reset
  - 0002H-000BH: Vector table to which address from which program is started is written after interrupt
  - 0020H-007FH: Table area referenced by GETI instruction

- Data memory (RAM)
  - Data area ....512 × 4 bits (000H–1FFH): μPD75108
    320 × 4 bits (000H-13FH) : μPD75106, 75104
  - Peripheral hardware area .... 128 × 4 bits (F80H–FFFH)

(a) μPD75108

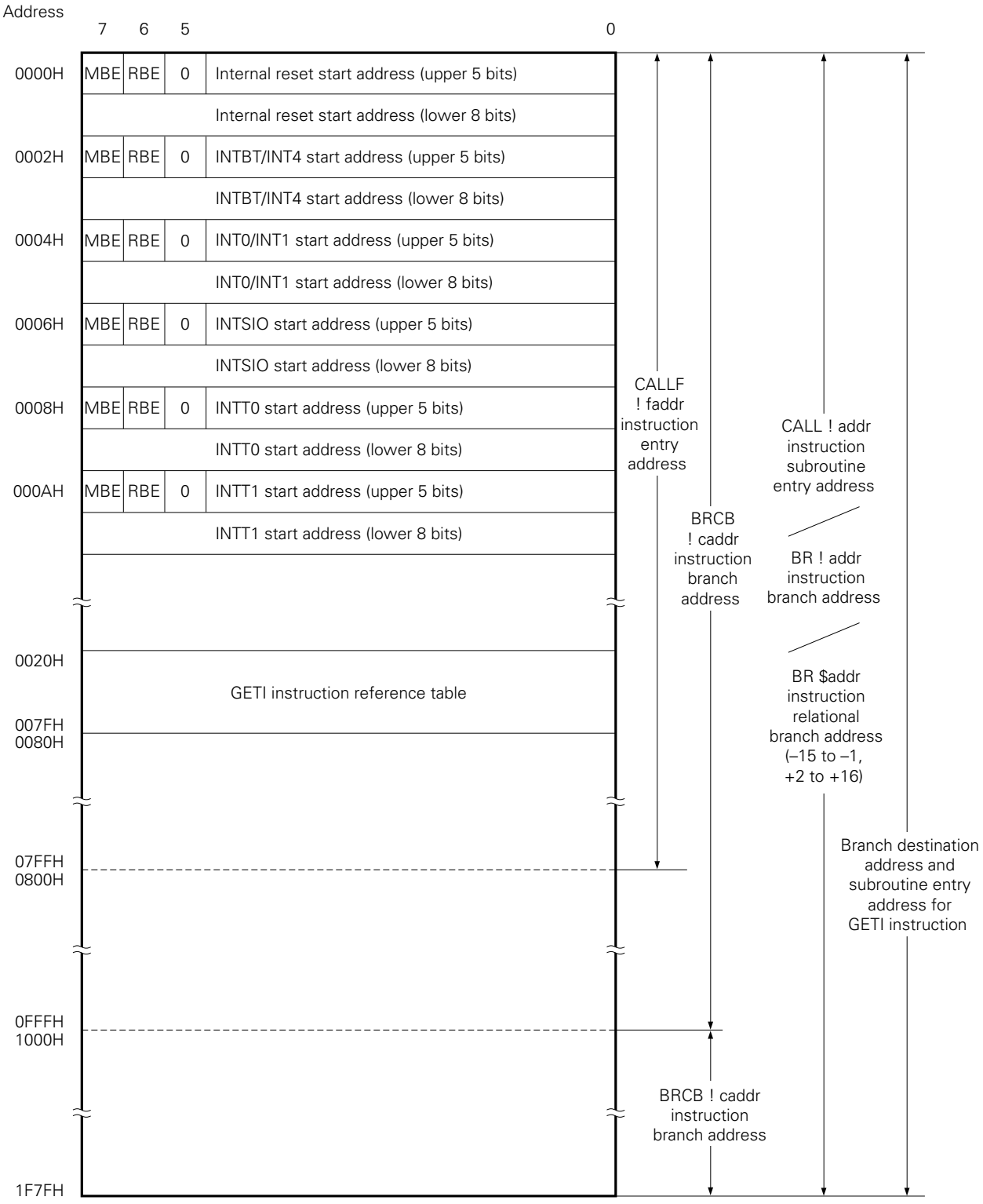


Fig. 4-1 Program Memory Map (1/3)

Remarks: In addition to the above addresses, program can be branched to addresses specified by the PC with the contents of its lower 8 bits changed by BR PCDE or BR PCXA instruction.

(b) μPD75106

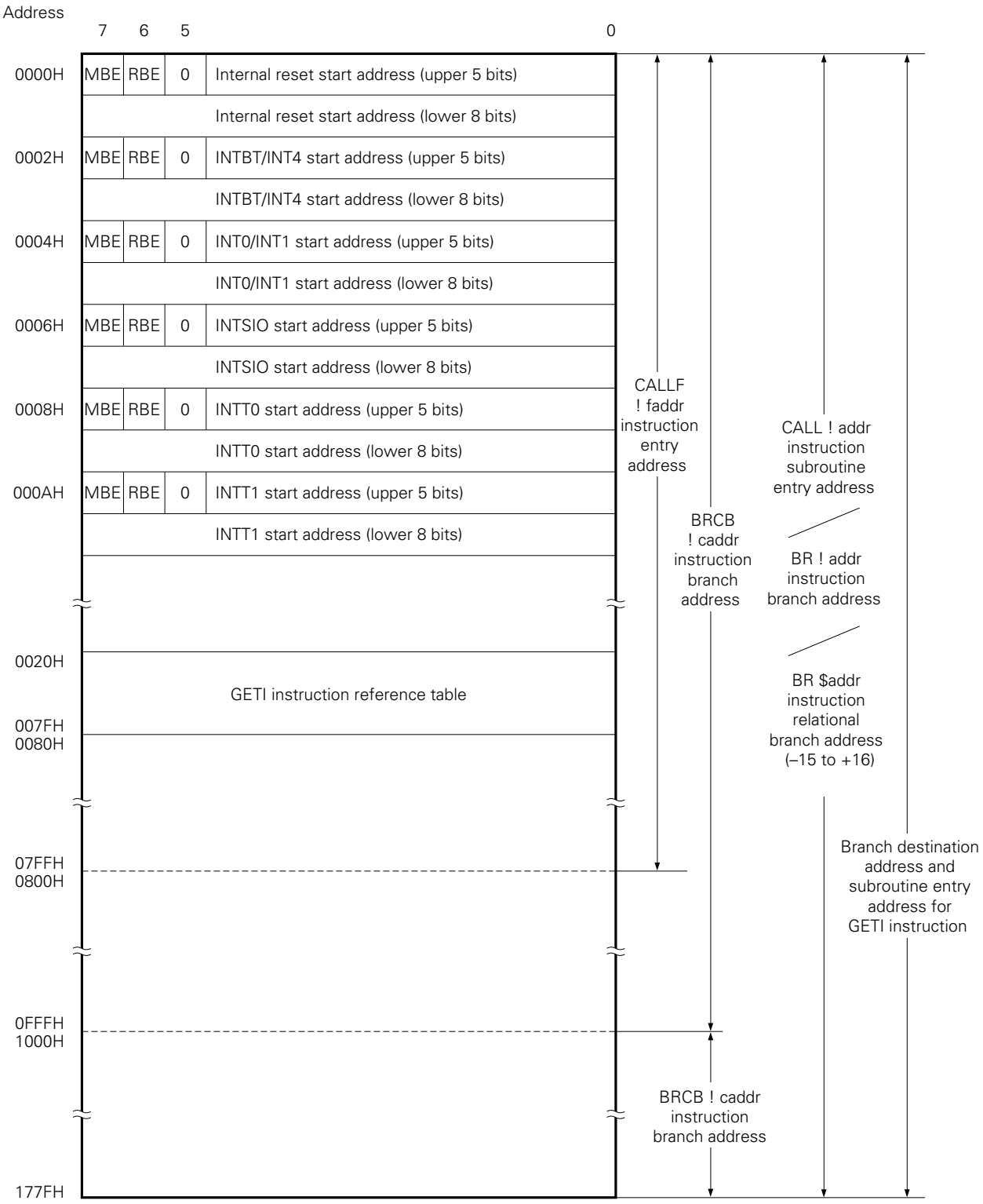


Fig. 4-1 Program Memory Map (2/3)

Remarks: In addition to the above addresses, program can be branched to addresses specified by the PC with the contents of its lower 8 bits changed by BR PCDE or BR PCXA instruction.

(c) μPD75106

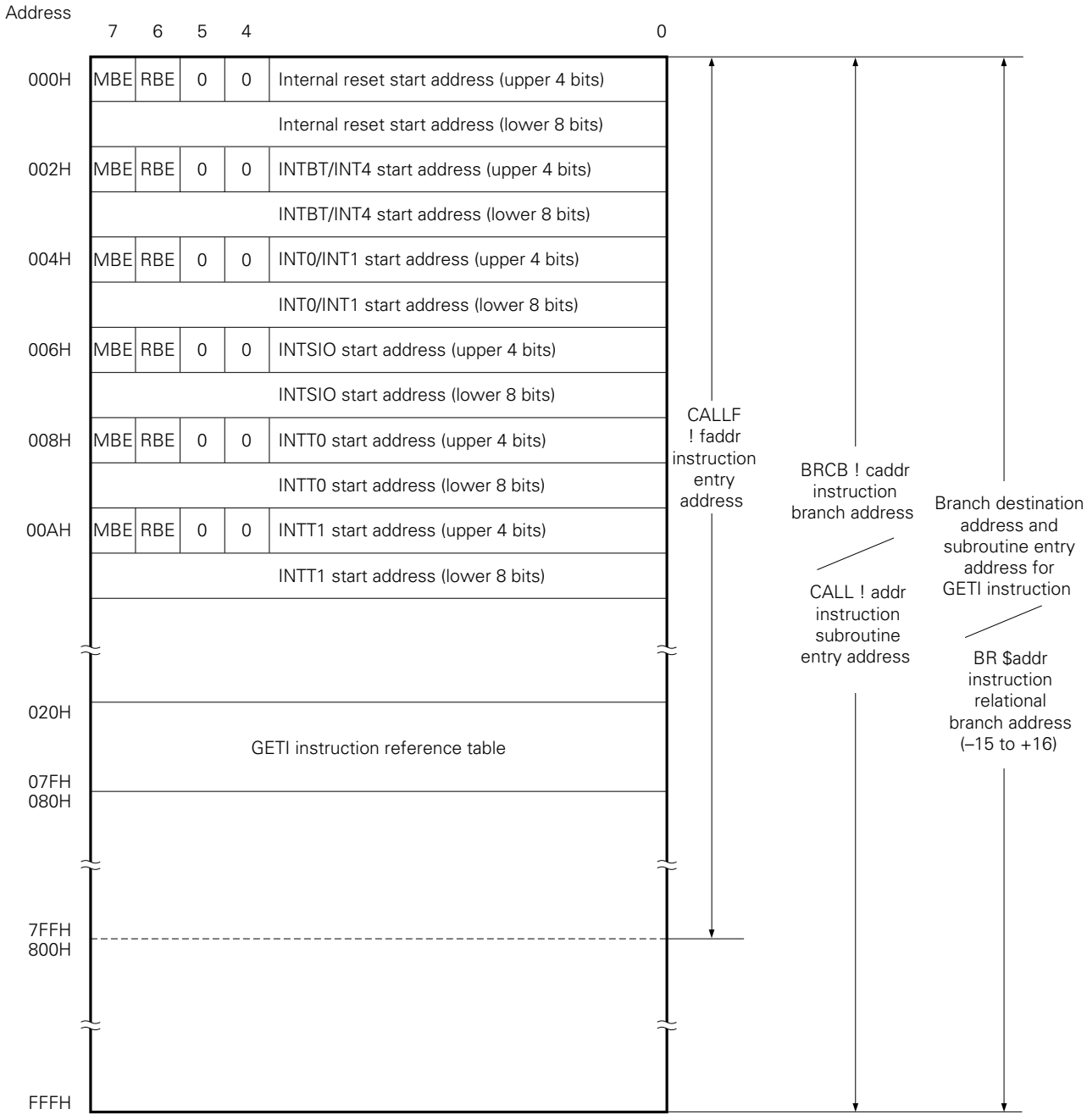


Fig. 4-1 Program Memory Map (3/3)

Remarks: In addition to the above addresses, program can be branched to addresses specified by the PC with the contents of its lower 8 bits changed by BR PCDE or BR PCXA instruction.

(a) μPD75108

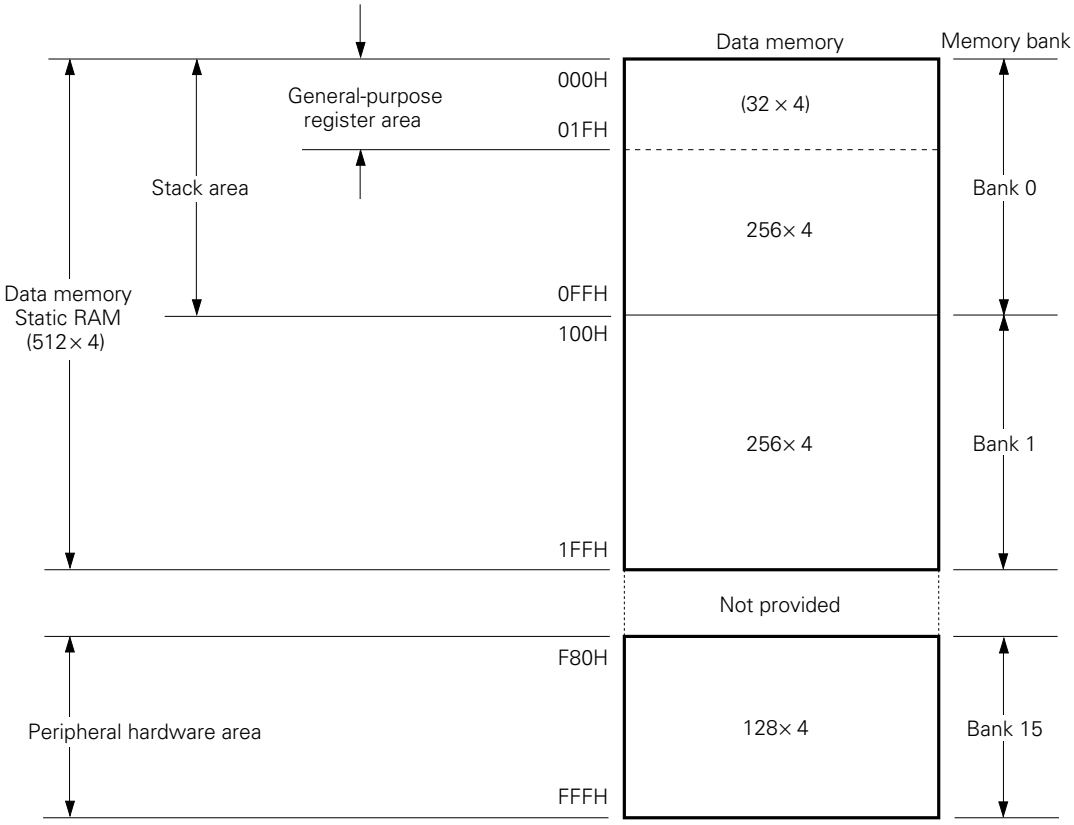


Fig. 4-2 Data Memory Map(1/2)

(b) μPD75106, 75104

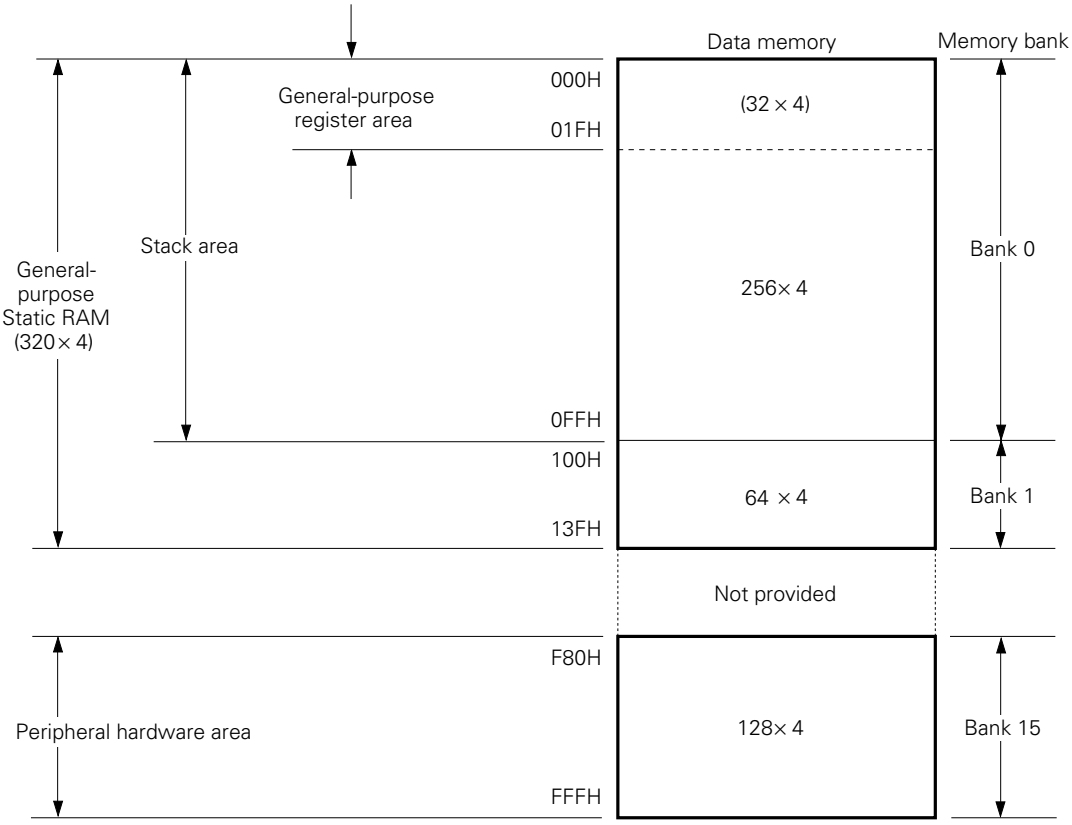


Fig. 4-2 Data Memory Map(2/2)

5. PERIPHERAL HARDWARE FUNCTIONS

5.1 PORTS

I/O ports are classified into the following 3 kinds:

- CMOS input (PORT0, 1) : 8
- CMOS input/output (PORT2, 3, 4, 5, 6, 7, 8, 9) : 32
- N-ch open-drain input/output (PORT12, 13, 14) : 12

Total : 52

Table 5-1 Port Function

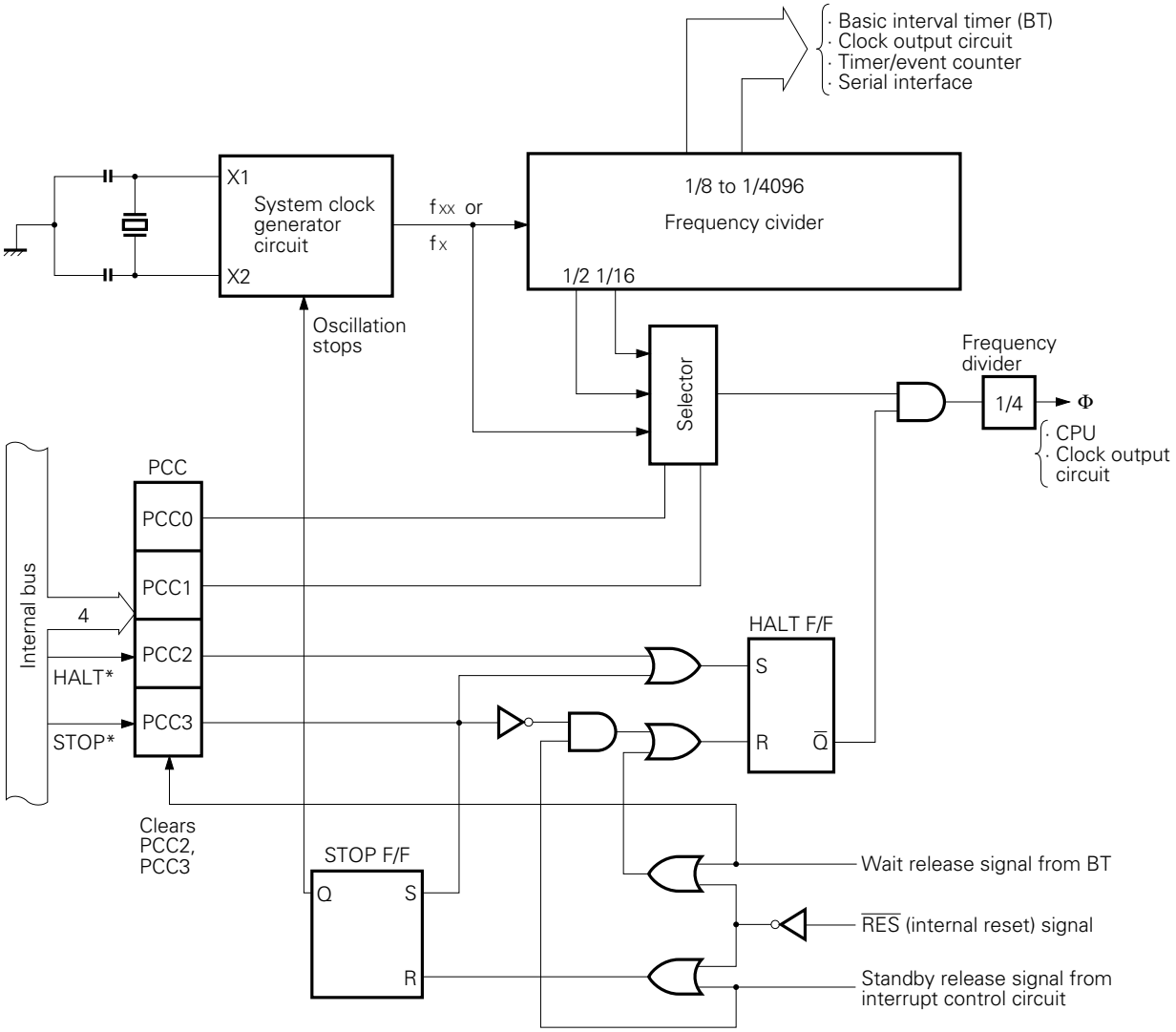
Port (Symbol)	Function	Operation and Features	Remarks
PORT0 PORT1	4-bit input	Can always be read or tested regardless of operation mode of shared pin	Shared with SI, SO, $\overline{SCK}$, and INT0 to 4 pins
PORT3 PORT6	4-bit I/O*	Can be set in input or output mode bitwise	—
PORT2 PORT4 PORT5 PORT7 PORT8 PORT9		Can be set in input or output mode in units of 4 bits. Ports 4 and 5, 6 and 7, 8 and 9 can be used in pairs to input or output 8-bit data	Port 2 pins are shared with PTO0, PTO1, and PCL pins
PORT12 PORT13 PORT14	4-bit I/O* (N-ch open- drain. 12V)	Can be set in input or output mode in units of 4 bits. Ports 12 and 13 can be used in pairs to input or output 8-bit data	Each bit can be connected to pull-up resistor by mask option

*: Can directly drive LED.

5.2 CLOCK GENERATOR CIRCUIT

The clock generator circuit generates clocks to control CPU operation modes by supplying clocks to the CPU and peripheral hardware. In addition, this circuit can change the instruction execution time.

- 0.95 μs/1.91 μs/15.3 μs (operating at 4.19 MHz)



*: Execution of the instruction

Remarks 1: f_{XX}= Crystal/ceramic oscillator

2: f_X = External clock frequency

3: PCC: Processor clock control register

4: One clock cycle (t_{CY}) of Φ is one machine cycle of an instruction. For t_{CY}, refer to AC characteristics in 12. ELECTRICAL SPECIFICATIONS. ★

Fig. 5-1 Clock Generator Block Diagram

5.3 CLOCK OUTPUT CIRCUIT

The clock output circuit outputs clock pulse from the P22/PCL pin. This clock output circuit is used to output clock pulses to the remote control output, peripheral LSIs, etc.

- Clock output (PCL) : Φ, 524, 262 kHz (operating at 4.19 MHz)

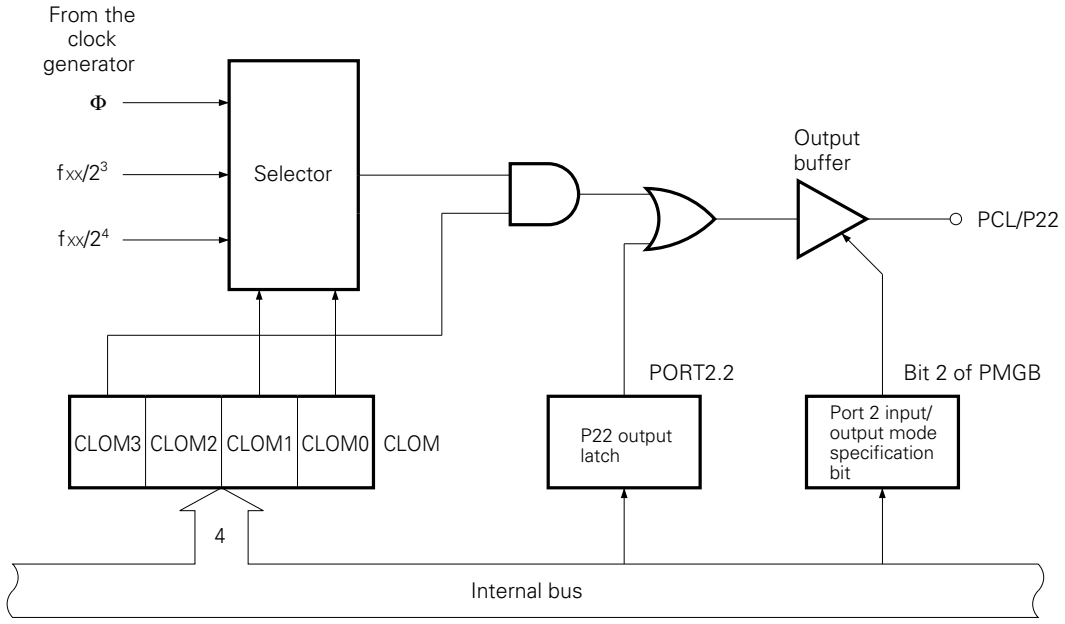
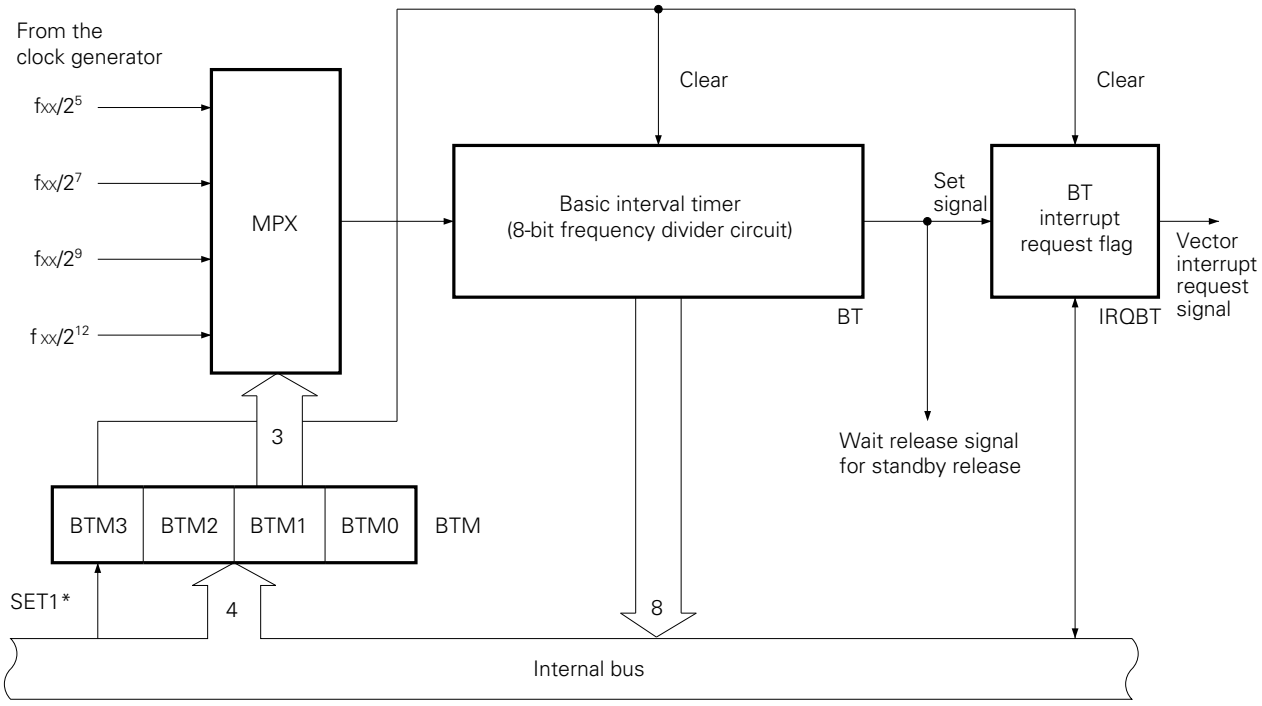


Fig. 5-2 Clock Output Circuit Configuration

5.4 BASIC INTERVAL TIMER

The basic interval timer has these functions:

- Interval timer operation which generates a reference time interrupt
- Watchdog timer application which detects a program runaway
- Selects the wait time for releasing the standby mode and counts the wait time
- Reads out the count value



Remarks : *: Instruction execution

Fig. 5-3 Basic Interval Timer Configuration

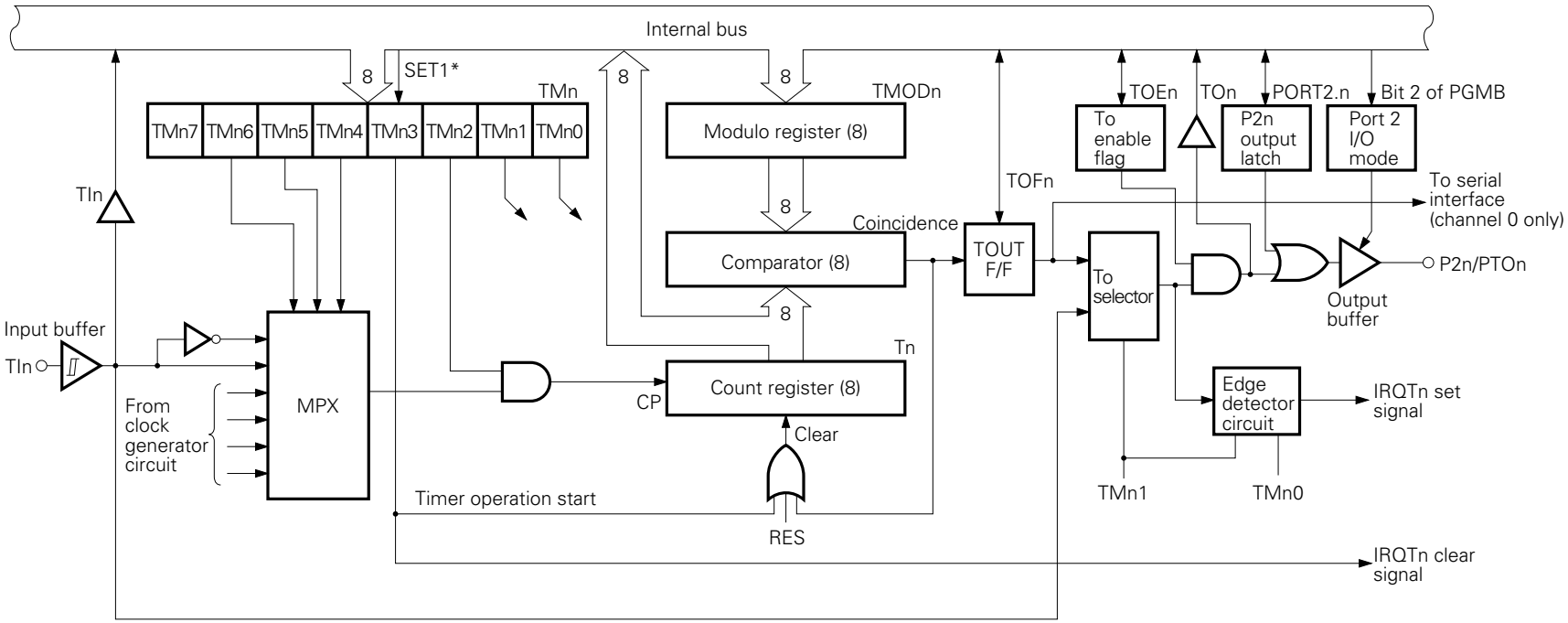
5.5 TIMER/EVENT COUNTER

μPD75108 contains two channels of timer/event counters.

These two channels are almost identical in terms of configuration and function except the count pulse (CP) that can be selected and the function to supply clocks to the serial interface.

The functions of the timer/event counter include:

- Programmable interval timer operation
- Output of square wave at an arbitrary frequency to PTOn pin
- Event counter operation
- Input of TIn pin signal as external interrupt input signal
- Dividing TIn pin input by N to output to PTOn pin (frequency divider operation)
- Supply of serial shift clock to serial interface circuit (channel 0 only)
- Reading counting status



Remarks: * indicates the instruction execution.

Fig. 5-4 Timer/Event Counter Block Diagram (n = 0, 1)

5.6 SERIAL INTERFACE

The μPD75108 is equipped with clock 8-bit serial interface that operates in the following two modes:

- Operation stop mode
- Three-line serial I/O mode

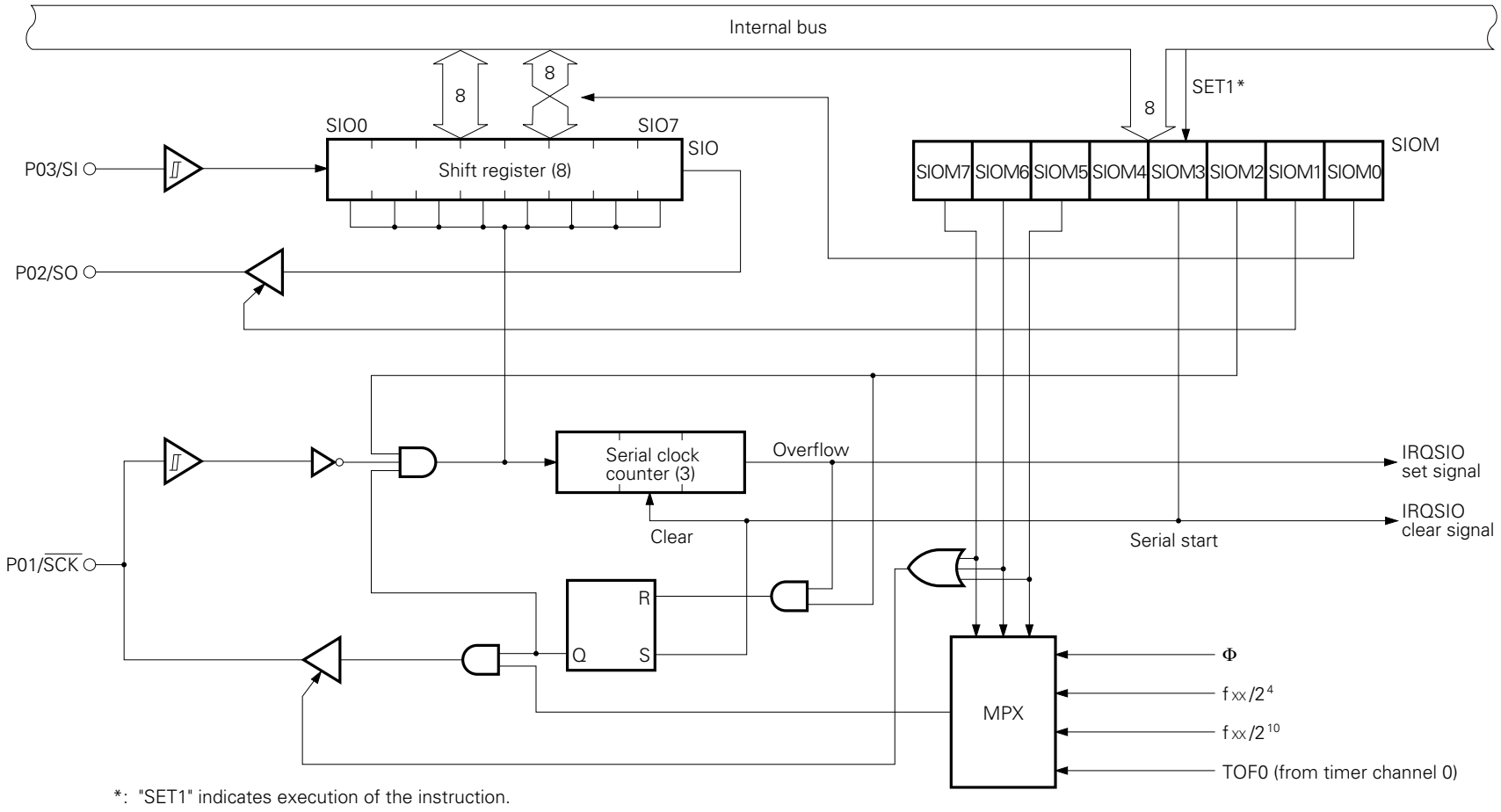


Fig. 5-5 Serial Interface Block Diagram

5.7 PROGRAMMABLE THRESHOLD PORT (ANALOG INPUT PORT)

μPD75108 is equipped with a 4-bit analog input port (consisting of PTH00 to PTH03 pins) whose threshold voltage is programmable.

This programmable threshold port is configured as shown in Figure 5-6.

The threshold voltage (V_{REF}) can be changed in 16 steps ($V_{DD} \times 0.5/16 - V_{DD} \times 15.5/16$), and analog signals can be directly input.

When V_{REF} is set to $V_{DD} \times 7.5/16$, the programmable threshold port can also be used as a digital signal input port.

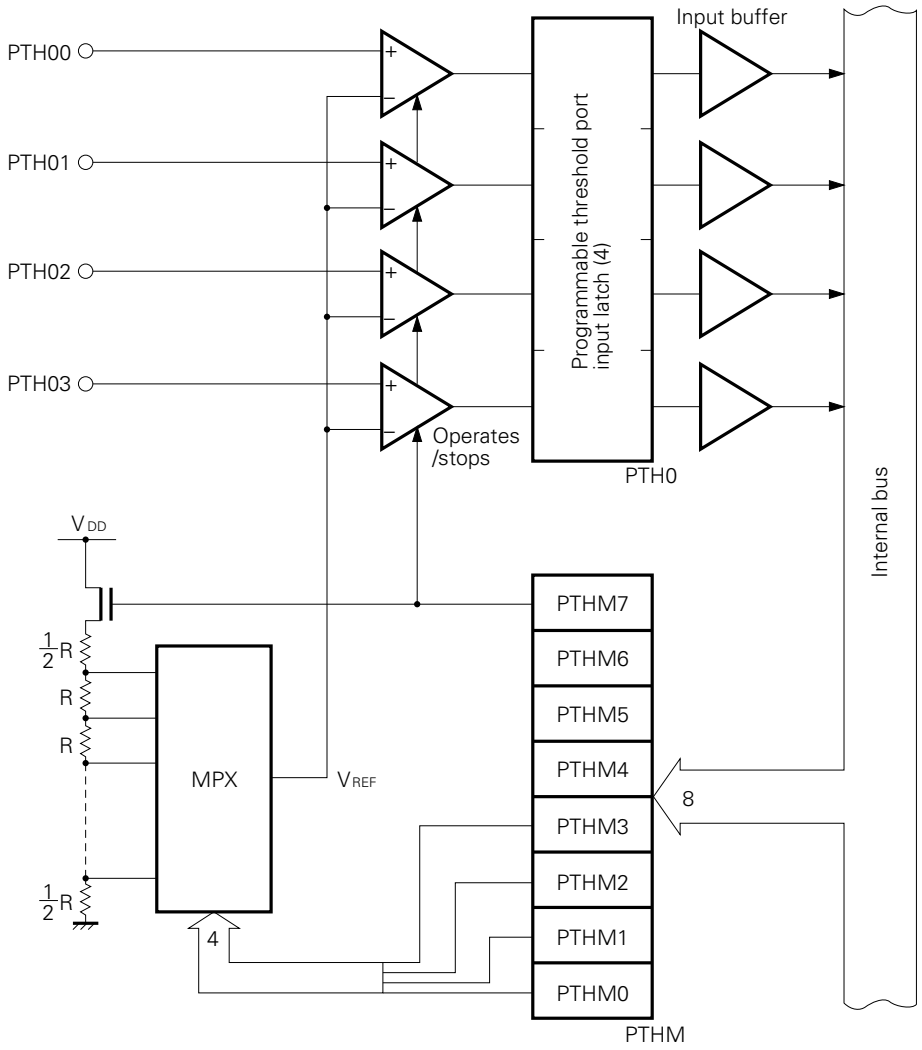
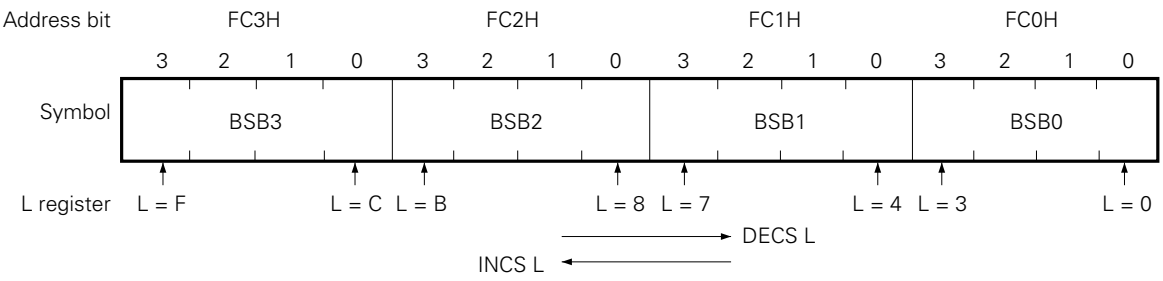


Fig. 5-6 Programmable Threshold Port Configuration

5.8 BIT SEQUENTIAL BUFFER .... 16 BITS

The bit sequential buffer is a data memory specifically provided for bit manipulation. With this buffer, addresses and bit specifications can be sequentially up-dated in bit manipulation operation. Therefore, this buffer is very useful for processing long data in bit units.



Remarks: For the pmem.@L addressing, the specification bit is shifted according to the L register.

Fig. 5-7 Bit Sequential Buffer Format

5.9 POWER-ON FLAG (MASK OPTION)

The power-ON flag (PONF) is set to only when the power-ON reset circuit operates and power-ON reset signal has been generated (see Fig. 8-1).

The PONF flag is mapped at bit 0 of memory space address FD1H, and can be manipulated by a bit manipulation instruction. However, it cannot be set by the SET1 instruction.

6. INTERRUPT FUNCTIONS

The μPD75108 has 7 different interrupt sources and can perform multiplexed interrupt processing with priority assigned.

In addition to that, the μPD75108 is also provided with two types of edge detection testable inputs.

The interrupt control circuit of the μPD75108 has these functions:

- Hardware controlled vector interrupt function which can control whether or not to accept an interrupt by using the interrupt enable flag (IExxx) and interrupt master enable flag (IME).
- The interrupt start address can be arbitrarily set.
- Multiplexed interrupt function that can specify priority by the interrupt priority selector register (IPS).
- Interrupt request flag (IRQxxx) test function (an interrupt generation can be confirmed by means of software).
- Standby mode release (Interrupts to be released can be selected by the interrupt enable flag).

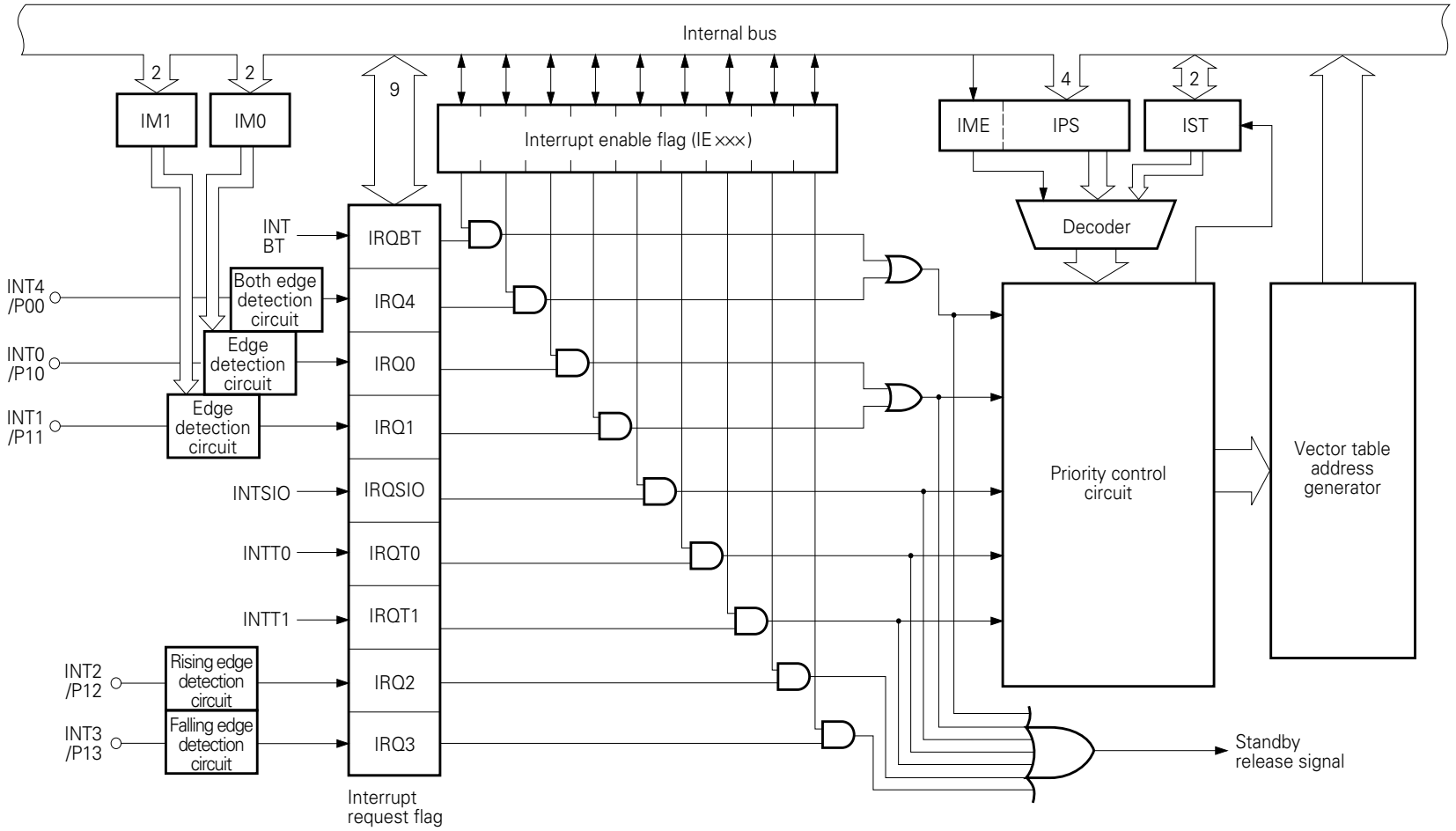


Fig. 6-1 Interrupt Control Block Diagram

7. STANDBY FUNCTIONS

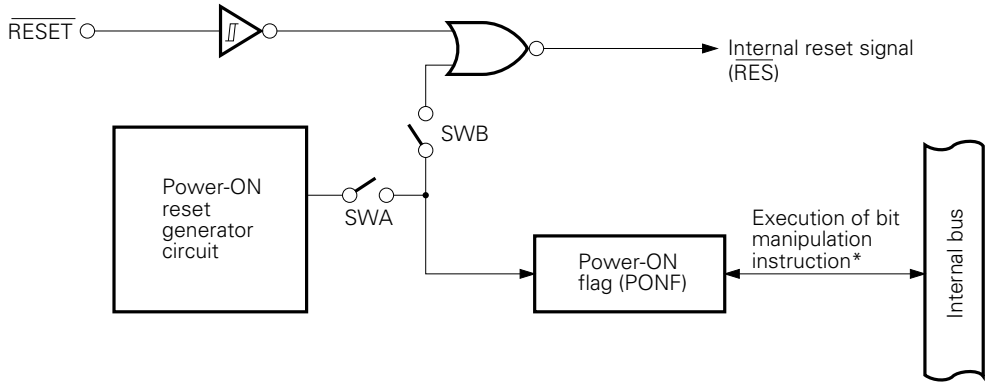
The μPD75108 has two different standby modes (STOP mode and HALT mode) to reduce the power consumption of the microcomputer chip while waiting for program execution.

Table 7-1 Each Status in Standby Mode

		STOP Mode	HALT Mode
Setting Instruction		STOP instruction	HALT instruction
Operation Status	Clock Generator circuit	Clock oscillation stops	Only CPU clock Φ is stopped
	Basic Interval Timer	Stops	Operates (sets IRQBT at reference time intervals)
	Serial Interface	Operates only when input of external $\overline{SCK}$ or output of TO0 is selected as serial clock (where external TI0 is input to timer/event counter 0)	Operates when serial clock other than Φ is specified
	Timer/Event Counter	Operates only when TIn pin input signal is specified as count clock	Operates
	Clock output circuit	Stops	Operates when clock other than CPU clock Φ is used
	CPU	Stops	Stops
Release Signal		Interrupt request signal enabled by interrupt enable flag, or $\overline{RESET}$ input	

8. RESET FUNCTION

The reset ($\overline{RES}$) signal generator circuit is configured as shown in Figure 8-1.

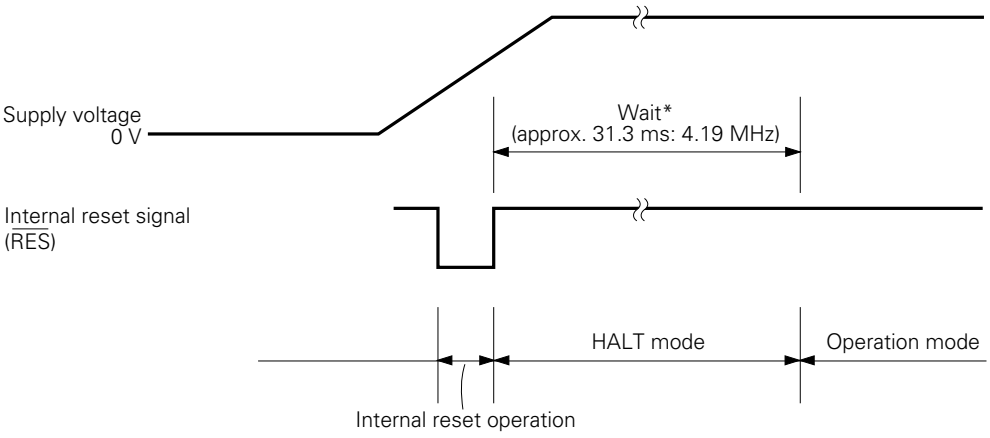


*: PONF cannot be set to 1 by SET1 instruction.

Fig. 8-1 Reset Signal Generator Circuit

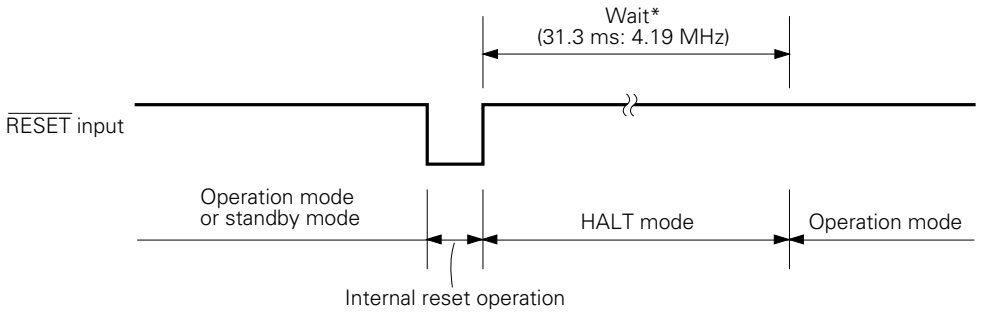
The Power-ON reset generator circuit generates an internal reset signal when the supply voltage rises. This pulse can be used in three ways by specifying a mask option through SWA and SWB shown in Fig. 8-1. (Refer to 11. MASK OPTION SELECTION.)

The reset operations performed by the Power-On reset circuit and the RESET input signal are illustrated in Figs. 8-2 and 8-3, respectively.



*: The wait time does not include the time required after the $\overline{RES}$ signal has been generated until the oscillation starts.

Fig. 8-2 Reset by Power-ON Reset Circuit



*: The wait time does not include the time required after the RES signal has been generated until the oscillation starts.

Fig. 8-3 Reset by RESET Signal

The status of each internal hardware device after the reset operation has been performed is shown in Table 8-1.

Table 8-1 Hardware Device Status After Reset

Hardware			$\overline{\text{RESET}}$ input during standby mode	Power-ON Reset or $\overline{\text{RESET}}$ Input during Operation
Program Counter (PC)			Lower 4 bits of program memory address 000H are set to PC_{12-8},*1 and contents of address 001H are set to PC_{7-0}.	Lower 4 bits of program memory address 000H are set to PC_{12-8},*1 and contents of address 001H are set to PC_{7-0}.
PSW	Carry Flag (CY)		Retained	Undefined
	Skip Flags (SK0-SK2)		0	0
	Interrupt Status Flags (IST0, 1)		0	0
	Bank Enable Flags (MBE, RBE)		Bit 6 of program memory address 000H is set in RBE, and bit 7 is set in MBE.	Bit 6 of program memory address 000H is set in RBE, and bit 7 is set in MBE.
Stack Pointer (SP)			Undefined	Undefined
Data Memory (RAM)			Retained*2	Undefined
General-Purpose Registers (X,A,H,L,D,E,B,C)			Retained	Undefined
Bank Selector Registers (MBS, RBS)			0, 0	0, 0
Basic interval timer		Counter (BT)	Undefined	Undefined
		Mode Register (BTM)	0	0
Timer/Event Counter (n = 0, 1)		Counter (Tn)	0	0
		Modulo Register (TMODn)	FFH	FFH
		Mode Register (TMn)	0	0
		TOEn, TOFn	0, 0	0, 0
Serial Interface		Shift Register (SIO)	Retained	Undefined
		Mode Register (SIOM)	0	0
Clock Generator Circuit, Clock Output Circuit		Processor Clock Control Register (PCC)	0	0
		Clock Output Mode Register (CLOM)	0	0
Interrupt		Interrupt Request Rlags (IRQxxx)	Reset (0)	Reset (0)
		Interrupt Enable Flags (IExxx)	0	0
		Priority Selector Register (IPS)	0	0
		INT0, 1 Mode Registers (IM0, IM1)	0, 0	0, 0
Digital Port		Output Buffer	OFF	OFF
		Output Latch	Cleared (0)	Cleared (0)
		I/O Mode Registers (PMGA, PMGB, PMGC)	0	0
Analog Port		PTH00-PTH03 Input Latches	Undefined	Undefined
		Mode Register (PTHM)	0	0
Power-ON Flag (PONF)			Retained	1 or undefined*2
Bit Sequential Buffer (BSB0-BSB3)			0	0

*1: PC_{11-8} for μPD75104

2: Power-ON reset: 1
$\overline{\text{RESET}}$ input during operation: undefined

Note: Data at data memory addresses 0F8H to 0FDH become undefined when the $\overline{\text{RESET}}$ signal has been input.

9. INSTRUCTION SET

(1) Operand representation and description

Describe one or more operands in the operand field of each instruction according to the operand representation and description methods of the instruction (for details, refer to RA75X Assembler Package User's Manual - Language (EEU-730)). With some instructions, only one operand should be selected from several operands. The uppercase characters, +, and – are keywords and must be described as is.

Describe an appropriate numeric value or label as immediate data.

The symbols in the register and flag symbols can be described as labels in the places of mem, fmem, pmem, and bit (for details, refer to μPD751XX Series User's Manual (IEM-922)). However, fmem and pmem restricts the label that can be described.

Representation	Description	
reg reg1	X, A, B, C, D, E, H, L X, B, C, D, E, H, L	
rp rp1 rp2 rp' rp'1	XA, BC, DE, HL BC, DE, HL BC, DE XA, BC, DE, HL, XA', BC', DE', HL' BC, DE, HL, XA', BC', DE', HL'	
rpa rpa1	HL, HL+, HL–, DE, DL DE, DL	
n4 n8	4-bit immediate data or label 8-bit immediate data or label	
mem bit	8-bit immediate data or label* 2-bit immediate data or label	
fmem pmem	FB0H to FBFH,FF0H to FFFH immediate data or label FC0H to FFFH immediate data or label	
addr	μPD75104	0000H to 0FFFH immediate data or label
	μPD75106	0000H to 177FH immediate data or label
	μPD75108	0000H to 1F7FH immediate data or label
caddr	12-bit immediate data or label	
faddr	11-bit immediate data or label	
taddr	20H to 7FH immediate data (where bit0 = 0) or label	
PORTn IExxx RBn MBn	PORT0 - PORT9, PORT12 - PORT14 IEBT, IESIO, IET0, IET1, IE0 - IE4 RB0 - RB3 MB0, MB1, MB15	

*: Only even address can be described as mem for 8-bit data processing.

(2) Legend of operation field

A	:	A register; 4-bit accumulator
B	:	B register; 4-bit accumulator
C	:	C register; 4-bit accumulator
D	:	D register; 4-bit accumulator
E	:	E register; 4-bit accumulator
H	:	H register; 4-bit accumulator
L	:	L register; 4-bit accumulator
X	:	X register; 4-bit accumulator
XA	:	Register pair (XA); 8-bit accumulator
BC	:	Register pair (BC); 8-bit accumulator
DE	:	Register pair (DE); 8-bit accumulator
HL	:	Register pair (HL); 8-bit accumulator
XA'	:	Expansion register pair (XA')
BC'	:	Expansion register pair (BC')
DE'	:	Expansion register pair (DE')
HL'	:	Expansion register pair (HL')
PC	:	Program counter
SP	:	Stack pointer
CY	:	Carry flag; or bit accumulator
PSW	:	Program status word
MBE	:	Memory bank enable flag
RBE	:	Register bank enable flag
PORTn	:	Port n (n = 0 - 9, 12 - 14)
IME	:	Interrupt mask enable flag
IPS	:	Interrupt priority selection register
IExxx	:	Interrupt enable flag
RBS	:	Register bank selection register
MBS	:	Memory bank selection register
PCC	:	Processor clock control register
·	:	Delimiter of address and bit
(xx)	:	Contents addressed by xx
xxH	:	Hexadecimal data

(3) Symbols in addressing area field

*1	MB = MBE · MBS (MBS = 0, 1, 15)		Data memory addressing
*2	MB = 0		
*3	MBE = 0 : MB = 0 (00H-7FH) MB = 15 (80H-FFH) MBE = 1 : MB = MBS (MBS = 0, 1, 15)		
*4	MB = 15, fmem = FB0H-FBFH, FF0H-FFFH		
*5	MB = 15, pmem = FC0H-FFFH		
*6	μPD75104	addr = 0000H-0FFFH	Program memory addressing
	μPD75106	addr = 0000H-177FH	
	μPD75108	addr = 0000H-1F7FH	
*7	addr = (Current PC) – 15 to (Current PC) – 1 (Current PC) + 2 to (Current PC) + 16		
*8	μPD75104	caddr = 0000H-0FFFH (PC_{11} = 0)	
	μPD75106	caddr = 0000H-0FFFH (PC_{12} = 0) or 1000H-177FH (PC_{12} = 1)	
	μPD75108	caddr = 0000H-0FFFH (PC_{12} = 0) or 1000H-1F7FH (PC_{12} = 1)	
*9	faddr = 000H-7FFH		
*10	taddr = 020H-07FH		

Remarks
- MB indicates memory bank that can be accessed.
- In *2, MB = 0 regardless of MBE and MBS.
- In *4 and *5, MB = 15 regardless of MBE and MBS.
- *6 to *10 indicate areas that can be addressed.

(4) Machine cycle field

In this field, S indicates the number of machine cycles required when an instruction having a skip function skips. The value of S varies as follows:

- When no instruction is skipped ..... S = 0
- When 1-byte or 2-byte instruction is skipped ..... S = 1
- When 3-byte instruction (BR ! adder or CALL ! adder) is skipped ..... S = 2

Note: The GETI instruction is skipped in one machine cycle.

One machine cycle equals to one cycle of the CPU clock Φ, (= t_{CY}), and can be changed in three steps depending on the setting of the processor clock control register (PCC).

Instructions	Mnemonics	Operand	Bytes	Machine Cycles	Operation	Addressing Area	Skip Conditions
Transfer	MOV	A, #n4	1	1	A ← n4		String effect A
		reg1, #n4	2	2	reg1 ← n4		
		XA, #n8	2	2	XA ← n8		String effect A
		HL, #n8	2	2	HL ← n8		String effect B
		rp2, #n8	2	2	rp2 ← n8		
		A, @HL	1	1	A ← (HL)	*1	
		A, @HL+	1	2+S	A ← (HL), then L ← L+1	*1	L = 0
		A, @HL–	1	2+S	A ← (HL), then L ← L–1	*1	L = FH
		A, @rpa1	1	1	A ← (rpa1)	*2	
		XA, @HL	2	2	XA ← (HL)	*1	
		@HL, A	1	1	(HL) ← A	*1	
		@HL, XA	2	2	(HL) ← XA	*1	
		A,mem	2	2	A ← (mem)	*3	
		XA, mem	2	2	XA ← (mem)	*3	
		mem, A	2	2	(mem) ← A	*3	
		mem, XA	2	2	(mem) ← XA	*3	
		A, reg	2	2	A ← reg		
		XA, rp'	2	2	XA ← rp'		
		reg1, A	2	2	reg1 ← A		
		rp'1, XA	2	2	rp'1 ← XA		
	XCH	A, @HL	1	1	A ↔ (HL)	*1	
		A, @HL+	1	2+S	A ↔ (HL), then L ← L+1	*1	L = 0
		A, @HL–	1	2+S	A ↔ (HL), then L ← L–1	*1	L = FH
		A, @rpa1	1	1	A ↔ (rpa1)	*2	
		XA, @HL	2	2	XA ↔ (HL)	*1	
		A, mem	2	2	A ↔ (mem)	*3	
		XA, mem	2	2	XA ↔ (mem)	*3	
		A, reg1	1	1	A ↔ reg1		
		XA, rp'	2	2	XA ↔ rp'		
Table Reference	MOVT	XA, @PCDE	1	3	• μPD75104 XA ← $(PC_{11-8}+DE)_{ROM}$ • μPD75106, 75108 XA ← $(PC_{12-8}+DE)_{ROM}$		
		XA, @PCXA	1	3	• μPD75104 XA ← $(PC_{11-8}+XA)_{ROM}$ • μPD75106, 75108 XA ← $(PC_{12-8}+XA)_{ROM}$		

Instructions	Mnemonics	Operand	Bytes	Machine Cycles	Operation	Addressing Area	Skip Conditions
Bit transfer	MOV1	CY,fmem.bit	2	2	CY ← (fmem.bit)	*4	
		CY,pmem.@L	2	2	CY ← ($pmem_{7-2}$+L_{3-2}.bit(L_{1-0}))	*5	
		CY,@H+mem.bit	2	2	CY ← (H+mem_{3-0}.bit)	*1	
		fmem.bit,CY	2	2	(fmem.bit) ← CY	*4	
		pmem.@L,CY	2	2	($pmem_{7-2}$+L_{3-2}.bit(L_{1-0})) ← CY	*5	
		@H+mem.bit, CY	2	2	(H+mem_{3-0}.bit) ← CY	*1	
Arithmetic operation	ADDS	A, #n4	1	1+S	A ← A+n4		carry
		XA, #n8	2	2+S	XA ← XA+n8		carry
		A, @HL	1	1+S	A ← A+(HL)	*1	carry
		XA, rp'	2	2+S	XA ← XA+rp'		carry
		rp'1, XA	2	2+S	rp'1 ← rp'1+XA		carry
	ADDC	A, @HL	1	1	A, CY ← A+(HL)+CY	*1	
		XA, rp'	2	2	XA, CY ← XA+rp'+CY		
		rp'1, XA	2	2	rp'1,CY ← rp'1+XA+CY		
	SUBS	A, @HL	1	1+S	A ← A-(HL).	*1	borrow
		XA, rp'	2	2+S	XA ← XA-rp'		borrow
		rp'1, XA	2	2+S	rp'1 ← rp'1-XA		borrow
	SUBC	A, @HL	1	1	A, CY ← A-(HL)-CY	*1	
		XA, rp'	2	2	XA, CY ← XA-rp'-CY		
		rp'1, XA	2	2	rp'1,CY ← rp'1-XA-CY		
	AND	A, #n4	2	2	A ← A ∧ n4		
		A, @HL	1	1	A ← A ∧ (HL)	*1	
		XA, rp'	2	2	XA ← XA ∧ rp'		
		rp'1, XA	2	2	rp'1 ← rp'1 ∧ XA		
	OR	A, #n4	2	2	A ← A ∨ n4		
		A, @HL	1	1	A ← A ∨ (HL)	*1	
		XA, rp'	2	2	XA ← XA ∨ rp'		
		rp'1, XA	2	2	rp'1 ← rp'1 ∨ XA		
	XOR	A, #n4	2	2	A ← A ⊻ n4		
		A, @HL	1	1	A ← A ⊻ (HL)	*1	
		XA, rp'	2	2	XA ← XA ⊻ rp'		
		rp'1, XA	2	2	rp'1 ← rp'1 ⊻ XA		
Accumulator Manipulation	RORC	A	1	1	CY ← A_0, A_3 ← CY, A_{n-1} ← A_n		
	NOT	A	2	2	A ← $\overline{A}$		
Increment/ decrement	INCS	reg	1	1+S	reg ← reg+1		reg = 0
		rp1	1	1+S	rp1 ← rp1+1		rp1 = 00H
		@HL	2	2+S	(HL) ← (HL)+1	*1	(HL) = 0
		mem	2	2+S	(mem) ← (mem)+1	*3	(mem) = 0
	DECS	reg	1	1+S	reg ← reg-1		reg = FH
		rp'	2	2+S	rp' ← rp'-1		rp' = FFH

Instructions	Mnemonics	Operand	Bytes	Machine Cycles	Operation	Addressing Area	Skip Conditions
Compare	SKE	reg, #n4	2	2+S	Skip if reg = n4		reg = n4
		@HL, #n4	2	2+S	Skip if (HL) = n4	*1	(HL) = n4
		A, @HL	1	1+S	Skip if A = (HL)	*1	A = (HL)
		XA, @HL	2	2+S	Skip if XA = (HL)	*1	XA = (HL)
		A, reg	2	2+S	Skip if A = reg		A = reg
		XA, rp'	2	2+S	Skip if XA = rp'		XA = rp'
Carry flag Manipulation	SET1	CY	1	1	CY ← 1		
	CLR1	CY	1	1	CY ← 0		
	SKT	CY	1	1+S	Skip if CY = 1		CY = 1
	NOT1	CY	1	1	CY ← $\overline{CY}$		
Memory/Bit Manipulation	SET1	mem.bit	2	2	(mem.bit) ← 1	*3	
		fmem.bit	2	2	(fmem.bit) ← 1	*4	
		pmem.@L	2	2	(pmem$_{7-2}$ + L$_{3-2}$.bit(L$_{1-0}$)) ← 1	*5	
		@H+mem.bit	2	2	(H + mem$_{3-0}$.bit) ← 1	*1	
	CLR1	mem.bit	2	2	(mem.bit) ← 0	*3	
		fmem.bit	2	2	(fmem.bit) ← 0	*4	
		pmem.@L	2	2	(pmem$_{7-2}$ + L$_{3-2}$.bit(L$_{1-0}$)) ← 0	*5	
		@H+mem.bit	2	2	(H+mem$_{3-0}$.bit) ← 0	*1	
	SKT	mem.bit	2	2+S	Skip if (mem.bit) = 1	*3	(mem.bit) = 1
		fmem.bit	2	2+S	Skip if (fmem.bit) = 1	*4	(fmem.bit) = 1
		pmem.@L	2	2+S	Skip if (pmem$_{7-2}$+L$_{3-2}$.bit (L$_{1-0}$)) = 1	*5	(pmem.@L) = 1
		@H+mem.bit	2	2+S	Skip if (H + mem$_{3-0}$.bit) = 1	*1	(@H+mem.bit) = 1
	SKF	mem.bit	2	2+S	Skip if (mem.bit) = 0	*3	(mem.bit) = 0
		fmem.bit	2	2+S	Skip if (fmem.bit) = 0	*4	(fmem.bit) = 0
		pmem.@L	2	2+S	Skip if (pmem$_{7-2}$ +L$_{3-2}$.bit (L$_{1-0}$)) = 0	*5	(pmem.@L) = 0
		@H+mem.bit	2	2+S	Skip if (H + mem$_{3-0}$.bit) = 0	*1	(@H+mem.bit) = 0
	SKTCLR	fmem.bit	2	2+S	Skip if (fmem.bit) = 1 and clear	*4	(fmem.bit) = 1
		pmem.@L	2	2+S	Skip if (pmem$_{7-2}$+L$_{3-2}$.bit (L$_{1-0}$)) = 1 and clear	*5	(pmem.@L) = 1
		@H+mem.bit	2	2+S	Skip if (H+mem$_{3-0}$.bit) = 1 and clear	*1	(@H+mem.bit) = 1
	AND1	CY,fmem.bit	2	2	CY ← CY ∧ (fmem.bit)	*4	
		CY,pmem.@L	2	2	CY ← CY ∧ (pmem$_{7-2}$+L$_{3-2}$.bit(L$_{1-0}$))	*5	
		CY,@H+mem.bit	2	2	CY ← CY ∧ (H+mem$_{3-0}$.bit)	*1	
	OR1	CY,fmem.bit	2	2	CY ← CY ∨ (fmem.bit)	*4	
		CY,pmem.@L	2	2	CY ← CY ∨ (pmem$_{7-2}$+L$_{3-2}$.bit (L$_{1-0}$))	*5	
		CY,@H+mem.bit	2	2	CY ← CY ∨ (H+mem$_{3-0}$.bit)	*1	
	XOR1	CY,fmem.bit	2	2	CY ← CY ⊻ (fmem.bit)	*4	
		CY,pmem.@L	2	2	CY ← CY ⊻ (pmem$_{7-2}$+L$_{3-2}$.bit (L$_{1-0}$))	*5	
		CY,@H+mem.bit	2	2	CY ← CY ⊻ (H+mem$_{3-0}$.bit)	*1	

Instructions	Mnemonics	Operand	Bytes	Machine Cycles	Operation	Addressing Area	Skip Conditions
Branch	BR	addr	—	—	• μPD75104 $PC_{11-0} \leftarrow$ addr (The most suitable instruction is selectable from among BRCB ! caddr, and BR $ addr depending on the assembler.)	*6	
					• μPD75106, 75108 $PC_{12-0} \leftarrow$ addr (The most suitable instruction is selectable from among BR ! addr, BRCB ! caddr, and BR $ addr depending on the assembler.)		
		! addr	3	3	• μPD75106, 75108 $PC_{12-0} \leftarrow$ addr	*6	
		$ addr	1	2	• μPD75104 $PC_{11-0} \leftarrow$ addr	*7	
					• μPD75106, 75108 $PC_{12-0} \leftarrow$ addr		
	BRCB	! caddr	2	2	• μPD75104 $PC_{11-0} \leftarrow caddr_{11-0}$	*8	
					• μPD75106, 75108 $PC_{12-0} \leftarrow PC_{12} + caddr_{11-0}$		
	BR	PCDE	2	3	• μPD75104 $PC_{11-0} \leftarrow PC_{11-8}$ + DE		
					• μPD75106, 75108 $PC_{12-0} \leftarrow PC_{12-8}$ + DE		
		PCXA	2	3	• μPD75104 $PC_{11-0} \leftarrow PC_{11-8}$ + XA		
					• μPD75106, 75108 $PC_{12-0} \leftarrow PC_{12-8}$ + XA		
Subroutine/ Stack Control	CALL	! addr	3	3	• μPD75104 $(SP-4)(SP-1)(SP-2) \leftarrow PC_{11-0}$ $(SP-3) \leftarrow$ MBE, RBE, 0, 0 $PC_{11-0} \leftarrow$ addr, SP ← SP-4	*6	
					• μPD75106, 75108 $(SP-4)(SP-1)(SP-2) \leftarrow PC_{11-0}$ $(SP-3) \leftarrow$ MBE, RBE, 0, PC_{12} $PC_{12-0} \leftarrow$ addr, SP ← SP-4		

Instructions	Mnemonics	Operand	Bytes	Machine Cycles	Operation	Addressing Area	Skip Conditions
Subroutine/ Stack Control (Cont'd)	CALLF	! faddr	2	2	• μPD75104 (SP-4)(SP-1)(SP-2) ← PC_{11-0} (SP-3) ← MBE, RBE, 0, 0 PC_{11-0} ←0, faddr, SP ← SP-4 • μPD75106, 75108 (SP-4)(SP-1)(SP-2) ← PC_{11-0} (SP-3) ← MBE, RBE, 0, PC_{12} PC_{12-0} ← 00, faddr, SP ← SP-4	*9	
	RET		1	3	• μPD75104 MBE, RBE, x, x ← (SP+1) PC_{11-0} ← (SP)(SP+3)(SP+2) SP ← SP+4 • μPD75106, 75108 MBE, RBE, x, PC_{12} ← (SP+1) PC_{11-0} ← (SP)(SP+3)(SP+2) SP ← SP+4		
	RETS		1	3+S	• μPD75104 MBE, RBE, x, x ← (SP+1) PC_{11-0} ← (SP)(SP+3)(SP+2) SP ← SP+4, then skip unconditionally • μPD75106, 75108 MBE, RBE, x, PC_{12} ← (SP+1) PC_{11-0} ← (SP)(SP+3)(SP+2) SP ← SP+4, then skip unconditionally		Unconditioned
	RETI		1	3	• μPD75104 MBE, RBE, x, x ← (SP+1) PC_{11-0} ← (SP)(SP+3)(SP+2) PSW ← (SP+4)(SP+5), SP ← SP+6 • μPD75106, 75108 MBE, RBE, x, PC_{12} ← (SP+1) PC_{11-0} ← (SP)(SP+3)(SP+2) PSW ← (SP+4)(SP+5), SP ← SP+6		
	PUSH	rp	1	1	(SP-1)(SP-2) ← rp, SP ← SP-2		
		BS	2	2	(SP-1) ← MBS, (SP-2) ← RBS, SP ← SP-2		
	POP	rp	1	1	rp ← (SP+1)(SP), SP ← SP+2		
		BS	2	2	MBS ← (SP+1), RBS ← (SP), SP ← SP+2		

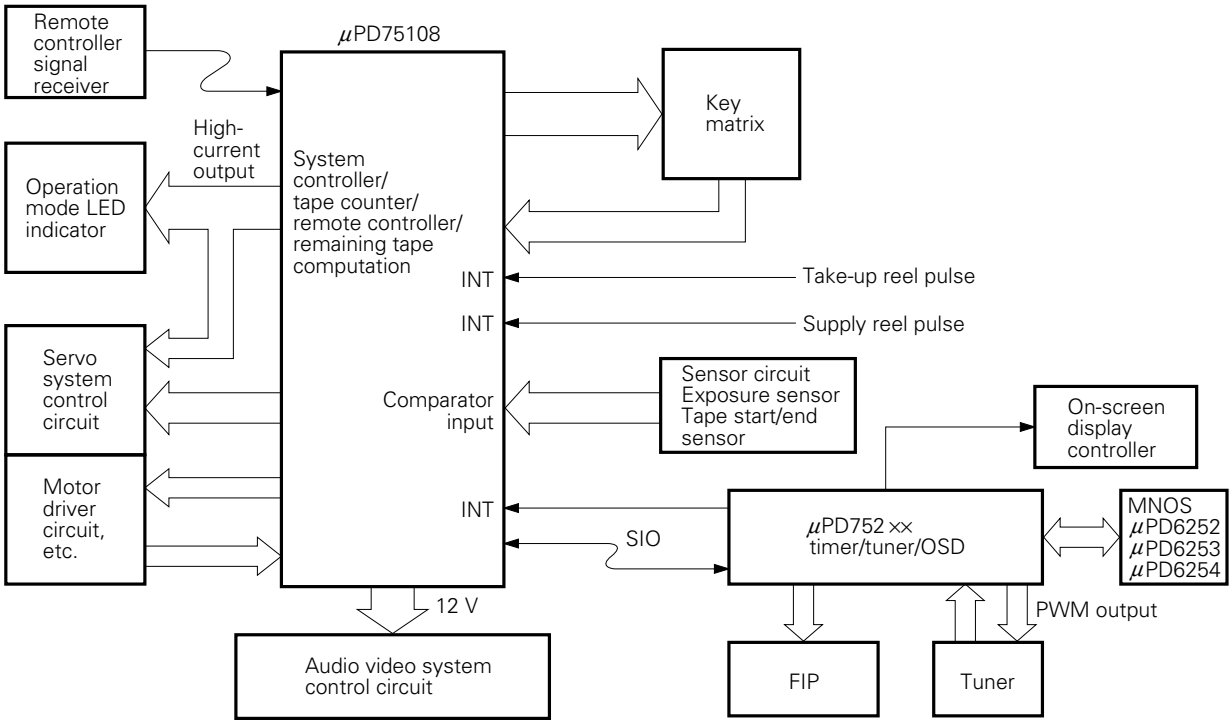
Instructions	Mnemonics	Operand	Bytes	Machine Cycles	Operation	Addressing Area	Skip Conditions
Interrupt Control	EI		2	2	IME (IPS.3) ← 1		
		IExxx	2	2	IExxx ← 1		
	DI		2	2	IME (IPS.3) ← 0		
		IExxx	2	2	IExxx ← 0		
I/O	IN*	A, PORTn	2	2	A ← $PORT_n$ (n = 0-9, 12-14)		
		XA, PORTn	2	2	XA ← $PORT_{n+1}$,$PORT_n$ (n = 4, 6, 8, 12)		
	OUT*	PORTn, A	2	2	$PORT_n$ ← A (n = 2-9, 12-14)		
		PORTn, XA	2	2	$PORT_{n+1}$, $PORT_n$ ← XA(n = 4, 6, 8, 12)		
CPU Control	HALT		2	2	Set HALT Mode (PCC.2 ← 1)		
	STOP		2	2	Set STOP Mode (PCC.3 ← 1)		
	NOP		1	1	No Operation		
Special	SEL	RBn	2	2	RBS ← n (n = 0-3)		
		MBn	2	2	MBS ← n (n = 0, 1, 15)		
	GETI	taddr	1	3	• μPD75104 • Where TBR instruction, PC_{11-0} ← $(taddr)_{3-0}$+(taddr+1)	*10	
					• Where TCALL instruction, (SP-4)(SP-1)(SP-2) ← PC_{11-0} (SP-3) ← MBE, RBE, 0, 0 PC_{11-0} ← $(taddr)_{3-0}$+(taddr+1) SP ← SP-4		
					• Except for TBR and TCALL instructions, Instruction execution of (taddr)(taddr+1)		Depends on referenced instruction
					• μPD75106, 75108 • Where TBR instruction, PC_{12-0} ← $(taddr)_{4-0}$+(taddr+1)		
					• Where TCALL instruction, (SP-4)(SP-1)(SP-2) ← PC_{11-0} (SP-3) ← MBE, RBE, 0, PC_{12} PC_{12-0} ← $(taddr)_{4-0}$+(taddr+1) SP ← SP-4		
					• Except for TBR and TCALL instructions, Instruction execution of (taddr)(taddr+1)		Depends on referenced instruction

*: When executing the IN/OUT instruction, MBE = 0, or MBE = 1, and MBS = 15.

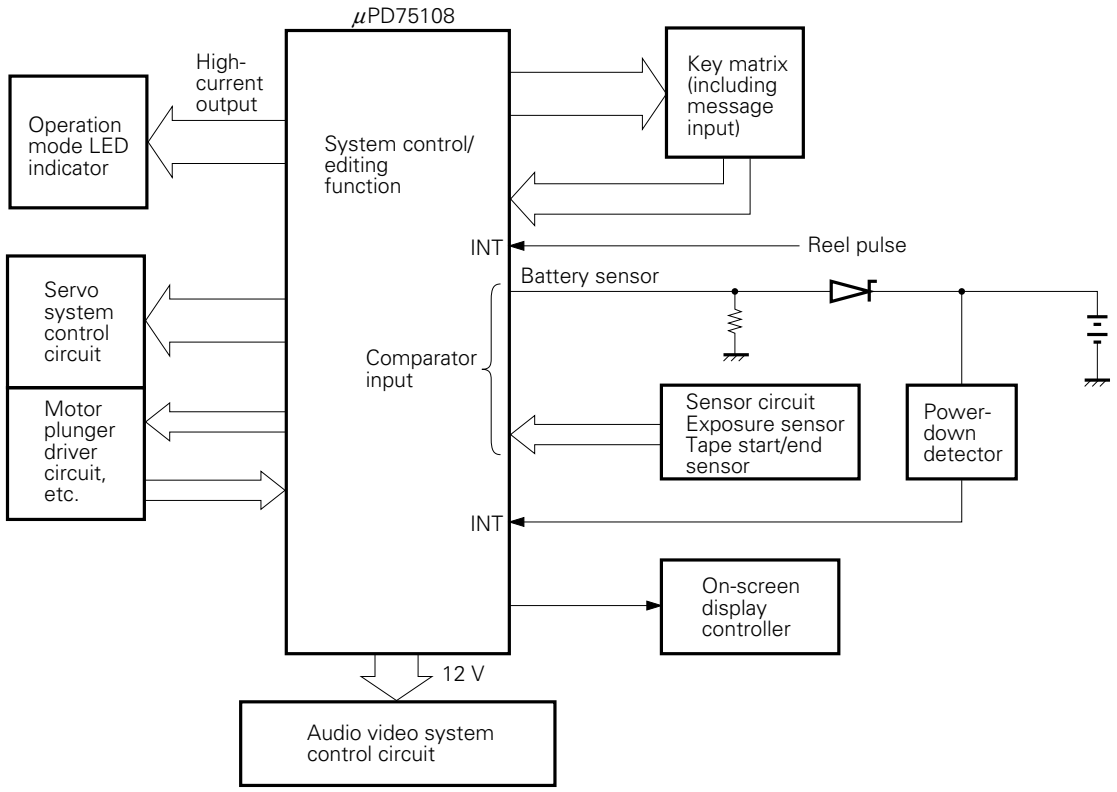
★ **Remarks:** TBR and TCALL instructions are assembler instructions for GETI instruction table definition.

10. APPLICATION EXAMPLES

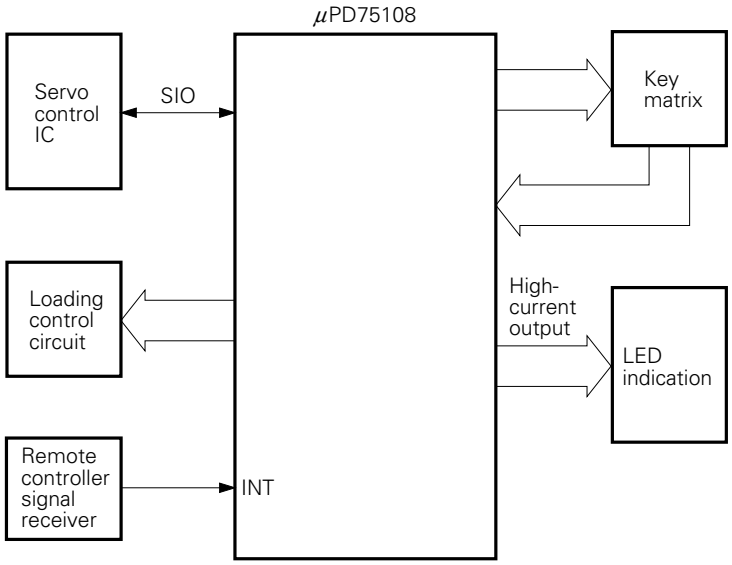
10.1 VTR SYSTEM CONTROLLER



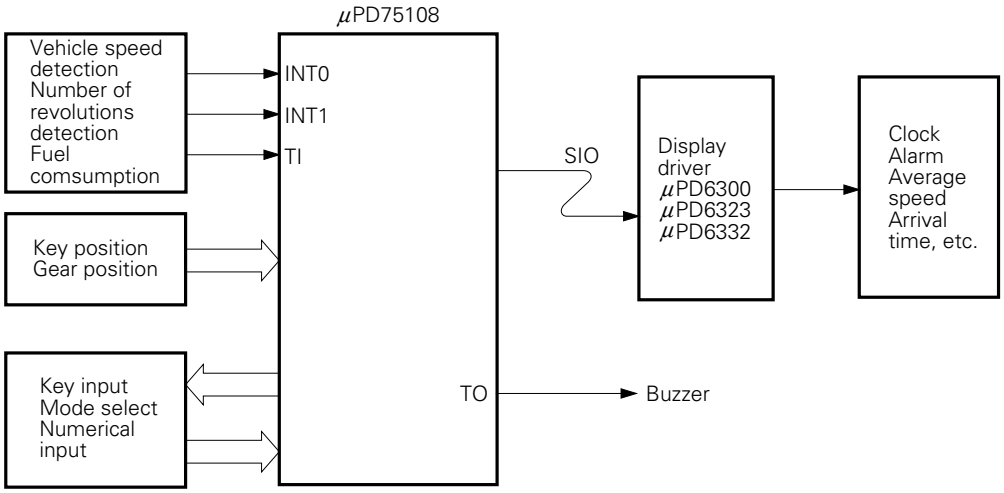
10.2 VTR CAMERA



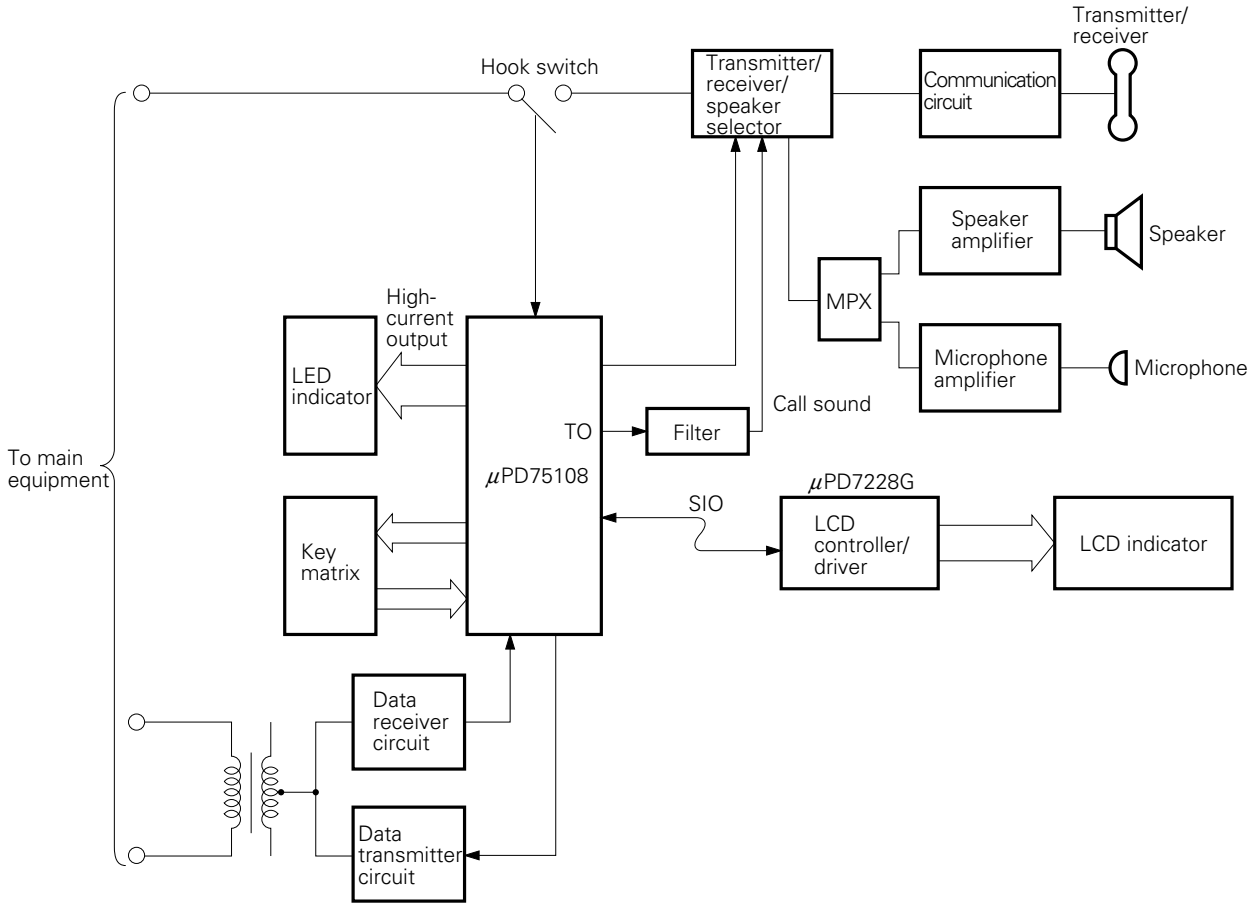
10.3 COMPACT DISC PLAYER



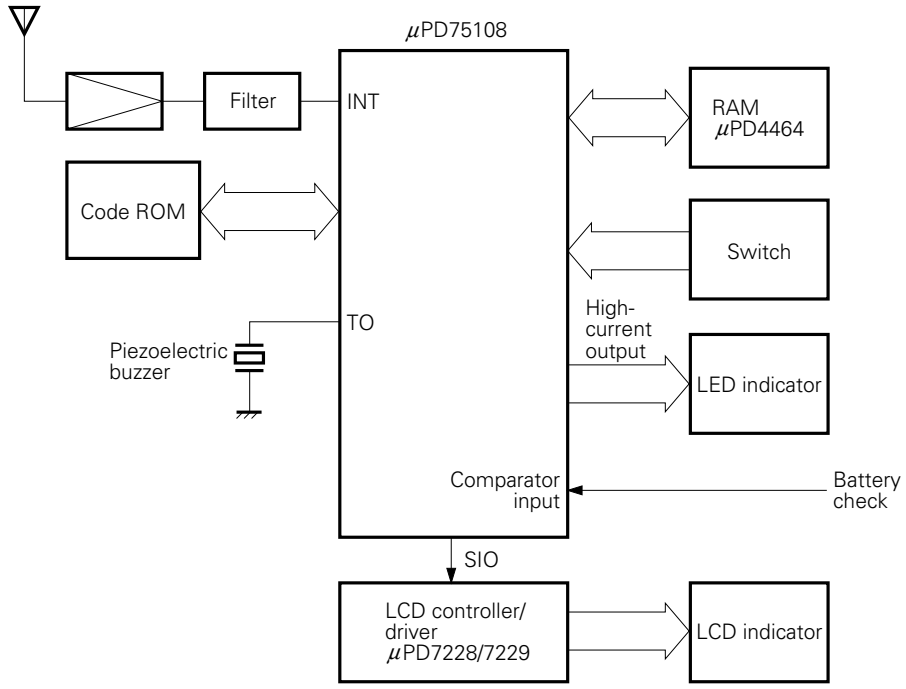
10.4 AUTOMOBILE APPLICATIONS (TRIP COMPUTER)



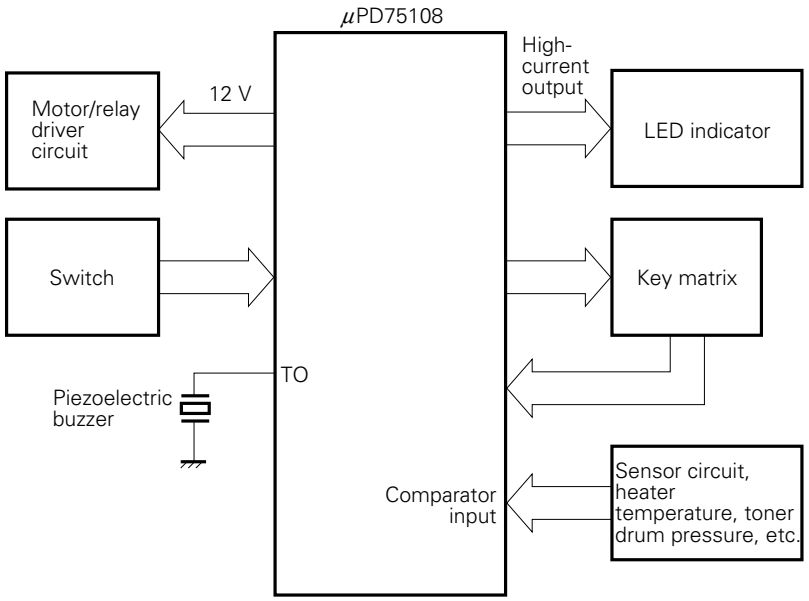
10.5 PUSHBUTTON TELEPHONE



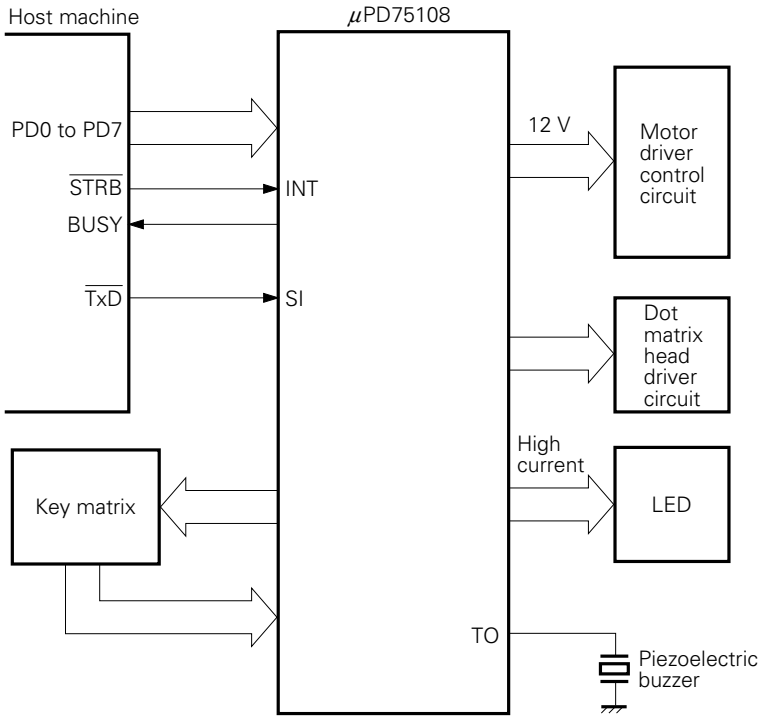
10.6 DISPLAY PAGER



10.7 PLAIN PAPER COPIER (PPC)



10.8 PRINTER CONTROLLER



11. MASK OPTION SELECTION

μPD75108 has the following mask options. Options to be built in can be selected.

(1) Pin

Pin	Mask Option
P120 - P123	Pull-down resistor can be built in bitwise.
P130 - P133	
P140 - P143	

(2) Power-ON reset generation circuit, power-ON flag (PONF)
One from the following three ways can be selected.

Switching Selection (Refer to Fig. 8-1.)		Power-On Reset Generation Circuit	Power-On Flag (PONF)	Internal Reset Signal ($\overline{RES}$)
SWA	SWB			
ON	ON	Provided	Provided	Generates automatically
ON	OFF	Provided	Provided	Not generates autoamtically
OFF	OFF	Not provided	Not provided	—

12. ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (T_a = 25°C)

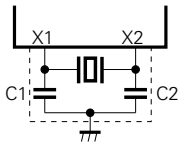
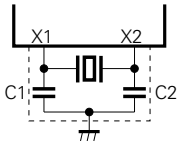
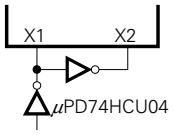
Parameter	Symbol	Conditions		Ratings	Unit
Supply Voltage	V_{DD}			-0.3 to +7.0	V
Input Voltage	V_{I1}	Other than ports 12, 13, 14		-0.3 to V_{DD}+0.3	V
	V_{I2}*1	Ports 12 to 14	w/pull-up resistor	-0.3 to V_{DD}+0.3	V
			Open drain	-0.3 to +13	V
Output Voltage	V_O			-0.3 to V_{DD}+0.3	V
High-Level Output Current	I_{OH}	1 pin		-15	mA
		All pins		-30	mA
Low-Level Output Current	I_{OL}*2	1 pin	Peak	30	mA
			rms	15	mA
		Total of ports 0, 2 to 4, 12 to 14	Peak	100	mA
			rms	60	mA
		Total of ports 5 to 9	Peak	100	mA
			rms	60	mA
Operating Temperature	T_{opt}			-40 to +85	°C
Storage Temperature	T_{stg}			-65 to +150	°C

*1: The power supply impedance (pull-up resistance) must be 50 kΩ or higher when a voltage higher than 10 V is applied to ports 12, 13, and 14.

2: rms = Peak value x $\sqrt{\text{Duty}}$

OSCILLATOR CIRCUIT CHARACTERISTICS

(T_a = -40 to +85°C, V_{DD} = 2.7 to 6.0 V)

Oscillator	Recommended Constants	Item	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic		Oscillation frequency(f_{XX})*1	V_{DD} = Oscillation voltage range	2.0		5.0*3	MHz
		Oscillation stabilization time*2	After V_{DD} come to MIN. of oscillation voltage range			4	ms
Crystal		Oscillation frequency (f_{XX})*1		2.0	4.19	5.0*3	MHz
		Oscillation stabilization time*2	V_{DD} = 4.5 to 6.0 V			10	ms
						30	ms
External Clock		X1 input frequency (f_X)*1		2.0		5.0*3	MHz
		X1 input high-, low-level widths (t_{XH}, t_{XL})		100		250	ns

*1: The oscillation frequency and X1 input frequency are indicated only to express the characteristics of the oscillator circuit. For instruction execution time, refer to AC Characteristics.

2: Time required for oscillation to stabilize after V_{DD} has come to MIN. of oscillation volrage range or the STOP mode has been released.

3: When the oscillation frequency is 4.19 MHz < fx ≤ 5.0 MHz, do not select PCC = 0011 as the instruction execution time: otherwise, one machine cycle is set to less than 0.95 μs, falling short of the rated minimum value of 0.95 μs. ★

Note: When using the oscillation circuit of the system clock, wire the portion enclosed in dotted line in the figures as follows to avoid adverse influences on the wiring capacity: ★

- Keep the wiring length as short as possible.
- Do not cross the wiring over the other signal lines. Also, do not route the wiring in the vicinity of lines through which a high alternating current flows.
- Always keep the ground point of the capacitor of the osccillator circuit at the same potential as V_{SS}. Do not connect the ground pattern through which a high current flows.
- Do not extract signals from the oscillation circuit.

RECOMMENDED OSCILLATOR CIRCUITS CONSTANTS

RECOMMENDED CERAMIC OSCILLATORS

Manufacturer	Product Name	External Capacitance (pF)		Oscillation Voltage Range (V)	
		C1	C2	MIN.	MAX.
Murata Mfg. Co., Ltd.	CSA 2.00MG	30	30	2.7	6.0
	CSA 4.19MG	30	30	3.0	6.0
	CSA 4.19MGU	30	30	2.7	6.0
	CST 4.19T	Provided	Provided	3.0	6.0
Kyoto Ceramic Co., Ltd.	KBR-2.0MS	100	100	3.0	6.0
	KBR-4.0MS	33	33	3.0	6.0
	KBR-4.19MS	33	33	3.0	6.0
	KBR-4.9152M	33	33	3.0	6.0

RECOMMENDED CRYSTAL OSCILLATOR

Manufacturer	Product Name	External Capacitance (pF)		Oscillation Voltage Range (V)	
		C1	C2	MIN.	MAX.
Kinseki	HC-49/U	22	22	2.7	6.0

DC CHARACTERISTICS (T_a = -40 to +85°C, V_{DD} = 2.7 to 6.0 V)

Item	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
High-Level Input Voltage	V_{IH1}	Other than below		0.7V_{DD}		V_{DD}	V
	V_{IH2}	Ports 0, 1, TI0, 1, $\overline{RESET}$		0.8 V_{DD}		V_{DD}	V
	V_{IH3}	Ports 12 to 14	Pull-up resistor	0.7 V_{DD}		V_{DD}	V
			Open drain	0.7 V_{DD}		12	V
	V_{IH4}	X1, X2		V_{DD}-0.5		V_{DD}	V
Low-Level Input Voltage	V_{IL1}	Other than below		0		0.3 V_{DD}	V
	V_{IL2}	Ports 0, 1, TI0, 1, $\overline{RESET}$		0		0.2 V_{DD}	V
	V_{IL3}	X1, X2		0		0.4	V
High-Level Output Voltage	V_{OH}	V_{DD} = 4.5 to 6.0 V,I_{OH} = -1 mA		V_{DD}-1.0			V
		I_{OH} = -100 μA		V_{DD}-0.5			V
Low-Level Output Voltage	V_{OL}	V_{DD} = 4.5 to 6.0 V	Ports 0, 2 to 9, I_{OL} = 15 mA		0.35	2.0	V
			Ports 12 to 14, I_{OL} = 10 mA		0.35	2.0	V
		V_{DD} = 4.5 to 6.0 V, I_{OL} = 1.6 mA				0.4	V
		I_{OL} = 400 μA				0.5	V
High-Level Input Leakage Current	I_{LIH1}	V_{IN} = V_{DD}	Other than below			3	μA
	I_{LIH2}		X1,X2			20	μA
	I_{LIH3}	V_{IN} = 12 V	Ports 12 to 14 (open drain)			20	μA
Low-Level Input Leakage Current	I_{LIL1}	V_{IN} = 0 V	Other than X1, X2			–3	μA
	I_{LIL2}		X1, X2			–20	μA
High-Level Output Leakage Current	I_{LOH1}	V_{OUT} = V_{DD}	Other than below			3	μA
	I_{LOH2}	V_{OUT} = 12 V	Ports 12 to 14 (open drain)			20	μA
Low-Level Output Leakage Current	I_{LOL}	V_{OUT} = 0 V				–3	μA
Internal Pull-Up Resistor*1	R_L	Ports 12 to 14	V_{DD} = 5 V±10%	15	40	70	kΩ
				10		80	kΩ
Supply Current*1	I_{DD1}	4.19MHz crystal oscillator C1 = C2 = 22pF	V_{DD} = 5 V±10%*2		3	9	mA
			V_{DD} = 3 V±10%*3		0.55	1.5	mA
	I_{DD2}		HALT mode V_{DD} = 5 V±10%		600	1800	μA
			HALT mode V_{DD} = 3±10%		200	600	μA
	I_{DD3}	STOP mode, V_{DD} = 3 V±10%			0.1	10	μA

*1: The current flowing into the internal pull-up resistor, power-ON reset circuit (mask option), and comparator circuit is not included.

2: When the high-speed mode is set by setting the processor clock control register (PCC) to 0011.

3: When the low-speed mode is set by setting the PCC to 0000.

CAPACITANCE (T_a = 25°C, V_{DD} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input Capacitance	C_{IN}	f = 1 MHz			15	pF
Output Capacitance	C_{OUT}	Pins other than thosemeasured are at 0 V			15	pF
Input/Output Capacitance	C_{IO}				15	pF

COMPARATOR CHARACTERISTICS (T_a = -40 to +85°C, V_{DD} = 4.5 to 6.0 V)

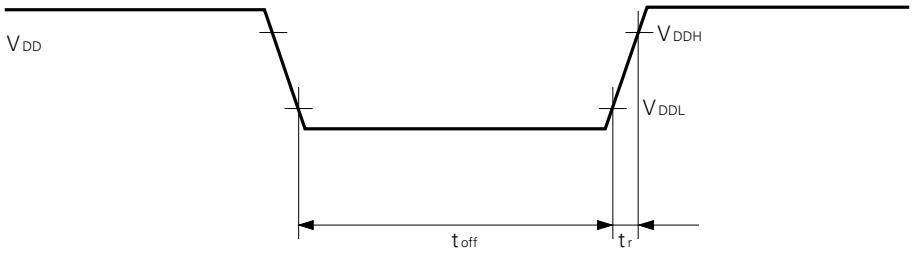
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Comparison Accuracy	V_{ACOMP}				±100	mV
Threshold Voltage	V_{TH}		0		V_{DD}	V
PTH Input voltage	V_{IPTH}		0		V_{DD}	V
Comparator circuit current dissipation		PTHM7 is set to "1"		1		mA

POWER-ON RESET CIRCUIT CHARACTERISTICS (MASK OPTION) (T_a = -40 to +85°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power-On Reset High-Level Operating Voltage	V_{DDH}		4.5		6.0	V
Power-On Reset Low-Level Operating Voltage	V_{DDL}		0		0.2	V
Supply Voltage Rise Time	t_r		10		*1	μs
Supply Voltage Off Time	t_{off}		1			s
Power-On Reset Circuit Current Dissipation*2	I_{DDPR}	V_{DD} = 5 V±10%		10	100	μA
		V_{DD} = 2.5 V		2	20	μA

*1: $2^{17}/f_{XX}$ (31.3 ms at f_{XX} = 4.19 MHz)

2: Current flowing when power-ON reset circuit or power-ON Flag is incorporeated.

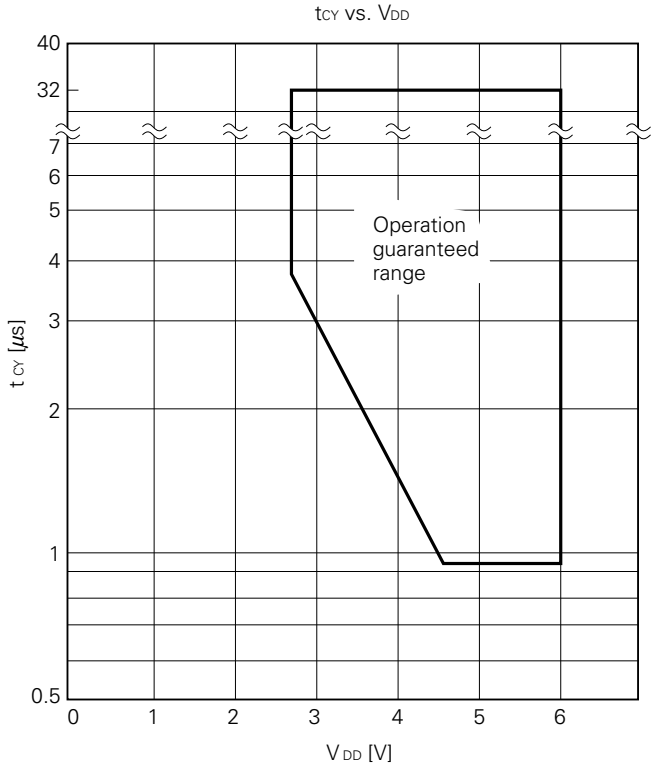


Note: Apply power gradually and smoothly.

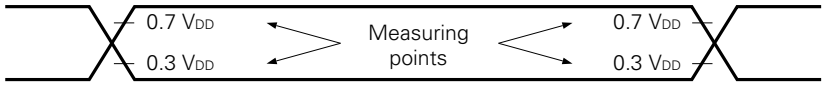
AC CHARACTERISTICS (T_a = -40 to +85°C, V_{DD} = 2.7 to 6.0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
CPU Clock Cycle Time* (Minimum Instruction Execution Time = 1 Machine Cycle)	t_{CY}	V_{DD} = 4.5 to 6.0 V		0.95		32	μs
				3.8		32	μs
TI0, TI1 Input Frequency	f_{TI}	V_{DD} = 4.5 to 6.0 V		0		1	MHz
				0		275	kHz
TI0, TI1 Input High-/Low-Level Width	t_{TIH}, t_{TIL}	V_{DD} = 4.5 to 6.0 V		0.48			μs
				1.8			μs
$\overline{SCK}$ Cycle Time	t_{KCY}	V_{DD} = 4.5 to 6.0 V	Input	0.8			μs
			Output	0.95			μs
			Input	3.2			μs
			Output	3.8			μs
$\overline{SCK}$ High-/Low-Level Width	t_{KH}, t_{KL}	V_{DD} = 4.5 to 6.0 V	Input	0.4			μs
			Output	t_{KCY}/2-50			ns
			Input	1.6			μs
			Output	t_{KCY}/2-150			ns
SI Setup Time (vs. $\overline{SCK}$↑)	t_{SIK}			100			ns
SI Hold Time (vs. $\overline{SCK}$↑)	t_{KSI}			400			ns
$\overline{SCK}$ ↓→ SO Output delay Time	t_{KSO}	V_{DD} = 4.5 to 6.0 V				300	ns
						1000	ns
INT0 to 4 High-/Low-Level Width	t_{INTH}, t_{INTL}			5			μs
$\overline{RESET}$ Low-Level Width	t_{RSL}			5			μs

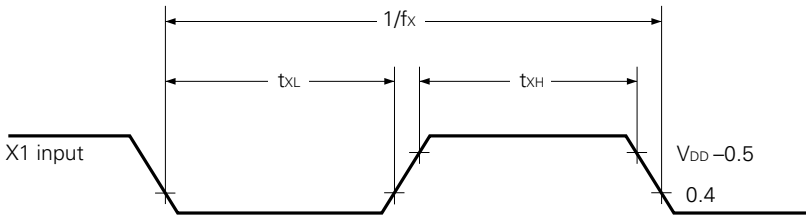
*: The cycle time of the CPU clock (Φ) is determined by the input frequency of the ceramic or crystal oscillator circuit and the set value of the processor clock control register. The t_{CY} vs. V_{DD} characteristics are as shown on the right.



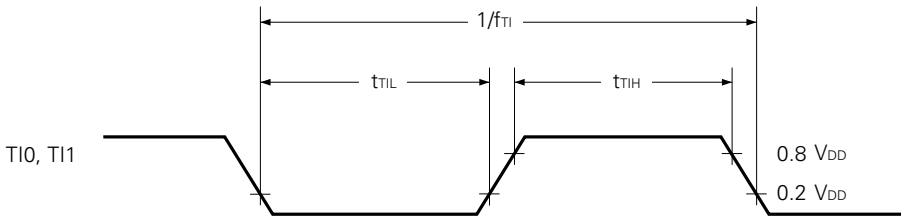
AC TIMING MEASURING POINTS (excluding Ports 0, 1, TI0, TI1, X1, X2, and $\overline{\text{RESET}}$)



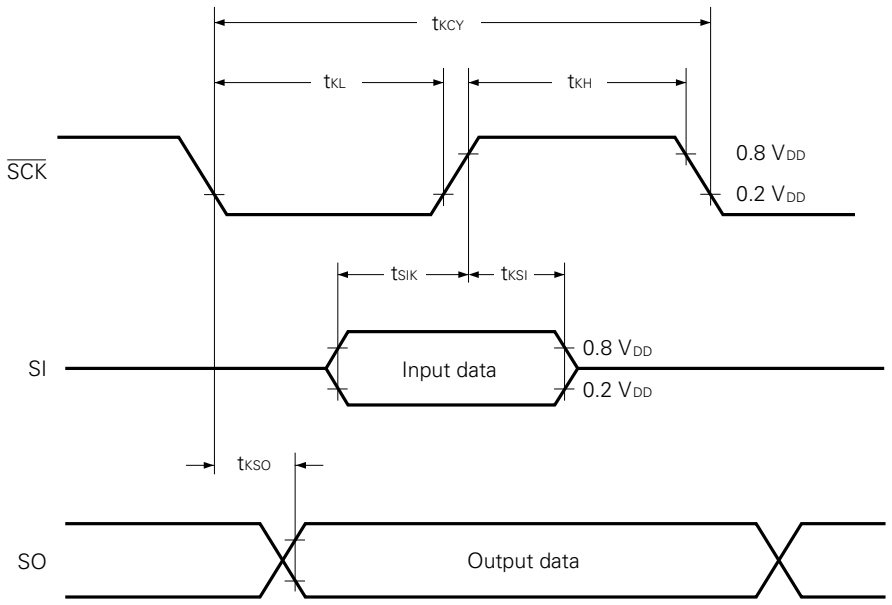
CLOCK TIMING



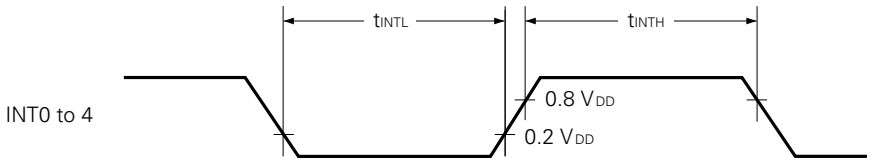
TI TIMING



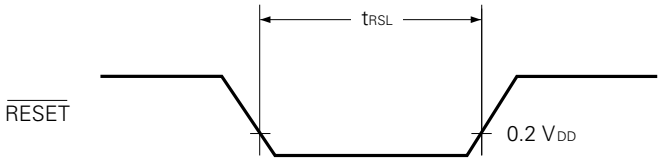
SERIAL TRANSFER TIMING



INTERRUPT INPUT TIMING



$\overline{\text{RESET}}$ INPUT TIMING



LOW-VOLTAGE DATA RETENTION CHARACTERISTICS OF DATA MEMORY IN STOP MODE

(T_a = −40 to +85°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data Retention Supply Voltage	V_{DDDR}		2.0		6.0	V
Data Retention Supply Current*1	I_{DDDR}	V_{DDDR} = 2.0 V		0.1	10	μA
Release Signal Set Time	t_{SREL}		0			μs
Oscillation Stabilization Wait Time*2	t_{WAIT}	Released by $\overline{RESET}$		$2^{17}/f_X$		ms
		Released by interrupt request		*3		ms

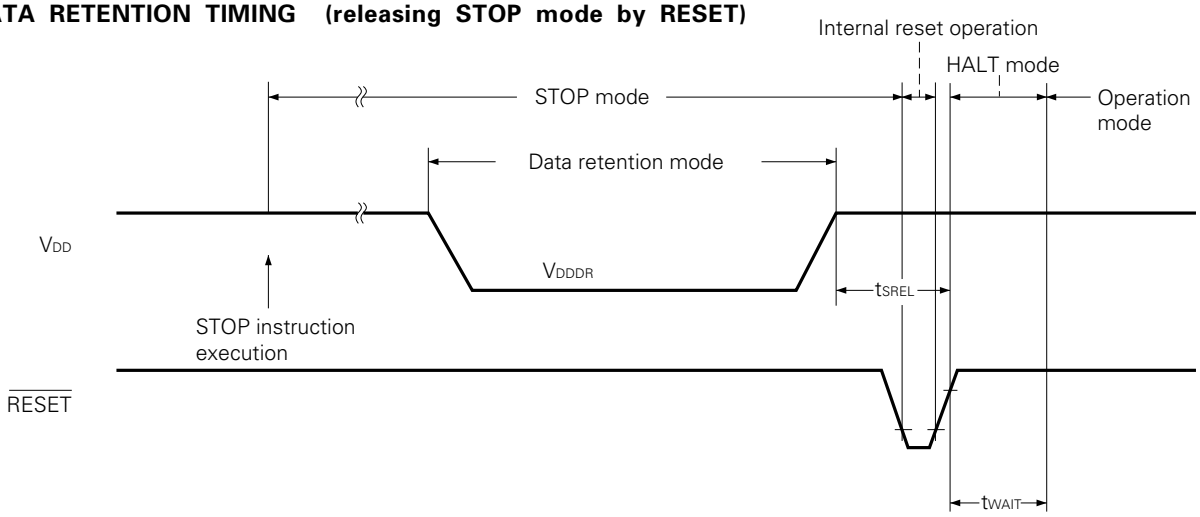
*1: The current flowing through internal pull-up resistor, power-ON reset circuit (mask option), and comparator circuit is not included

2: The oscillation stabilization wait time is the time during which the CPU is stopped to prevent unstable operation when oscillation is started.

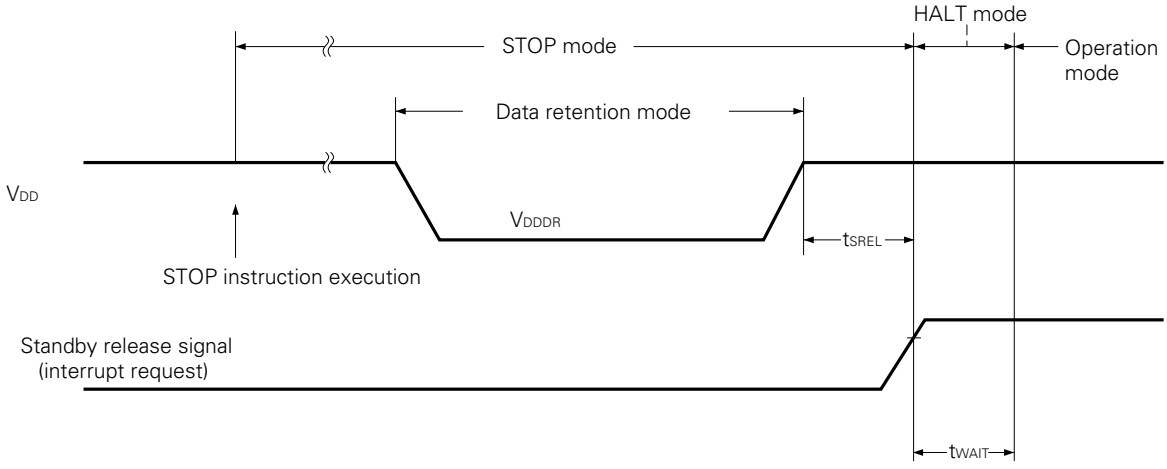
3: Depends on the setting of the basic interval timer mode register (BTM) as follows:

BTM3	BTM2	BTM1	BTM0	Wait time ( ): f_{XX} = 4.19 MHz
–	0	0	0	$2^{20}/f_{XX}$ (approx. 250 ms)
–	0	1	1	$2^{17}/f_{XX}$ (approx. 31.3 ms)
–	1	0	1	$2^{15}/f_{XX}$ (approx. 7.82 ms)
–	1	1	1	$2^{13}/f_{XX}$ (approx. 1.95 ms)

DATA RETENTION TIMING (releasing STOP mode by $\overline{RESET}$)

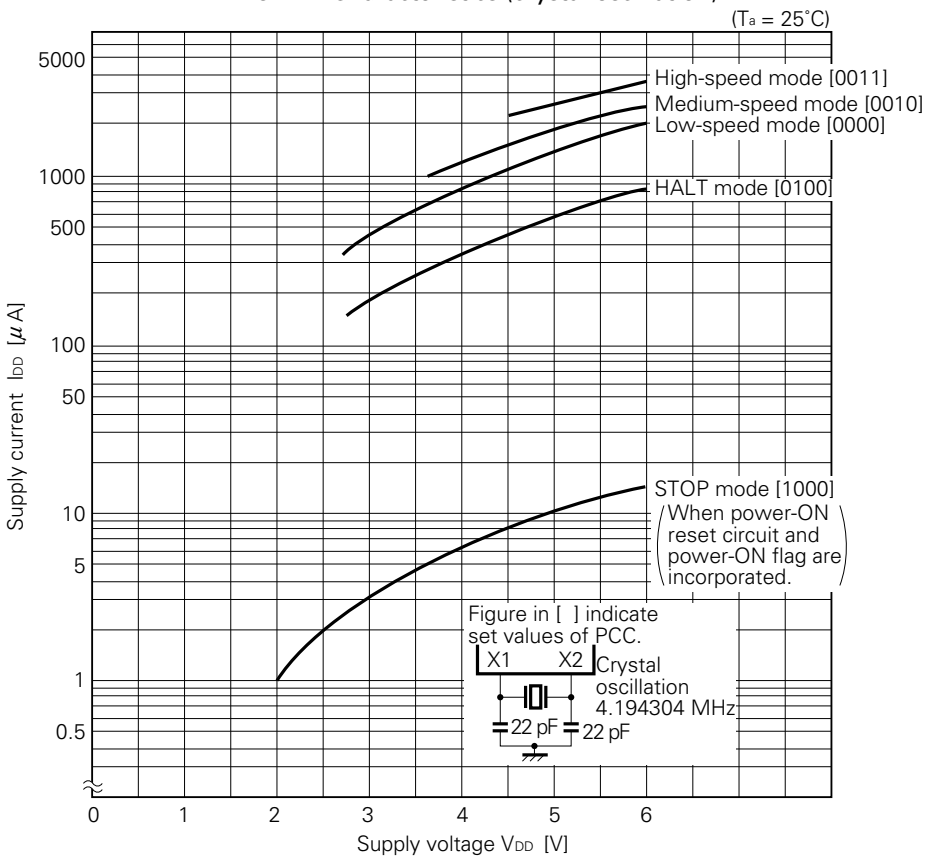


DATA RETENTION TIMING (standby release signal: releasing STOP mode by interrupt)

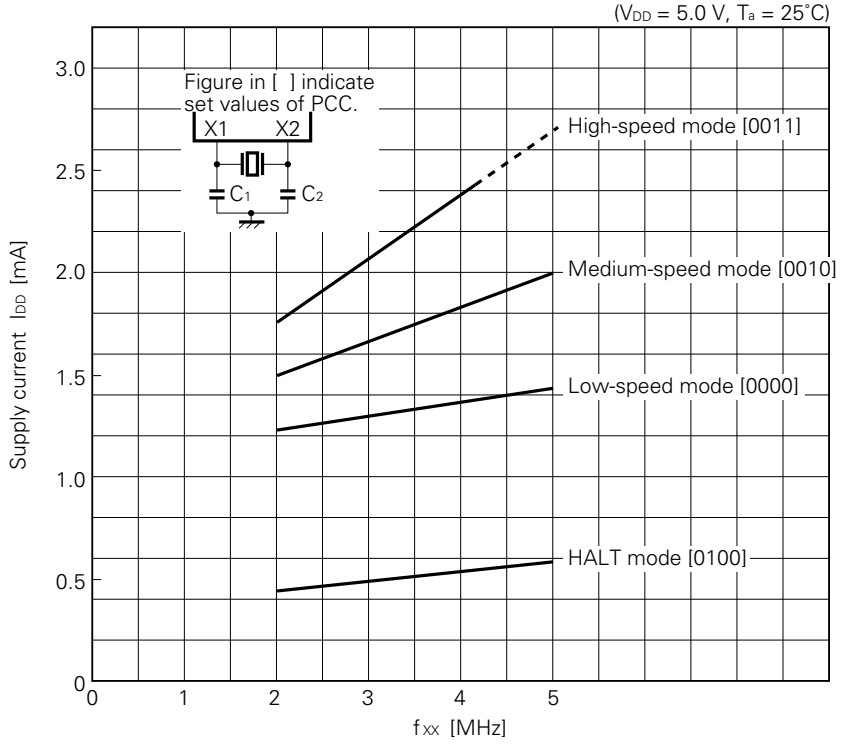


13. CHARACTERISTIC DATA

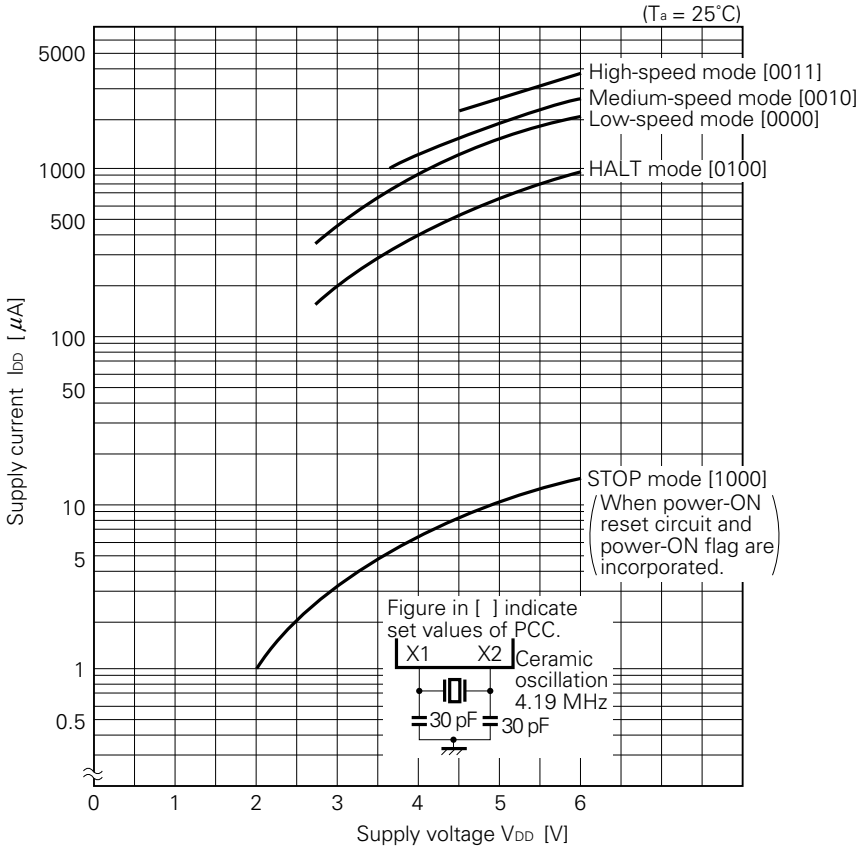
I_{DD} vs. V_{DD} Characteristics (crystal oscillation)



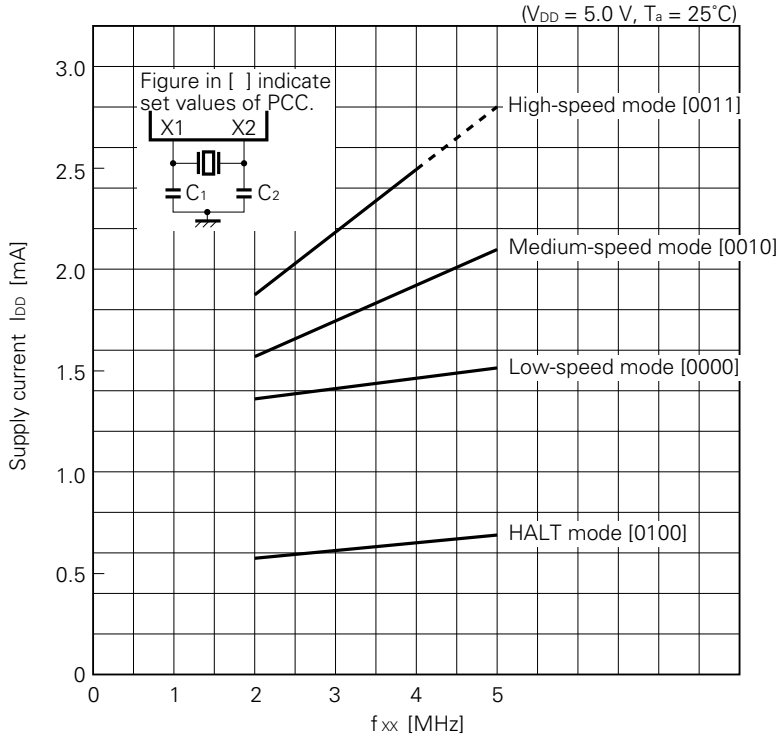
I_{DD} vs. f_{XX} Characteristics (crystal oscillation)



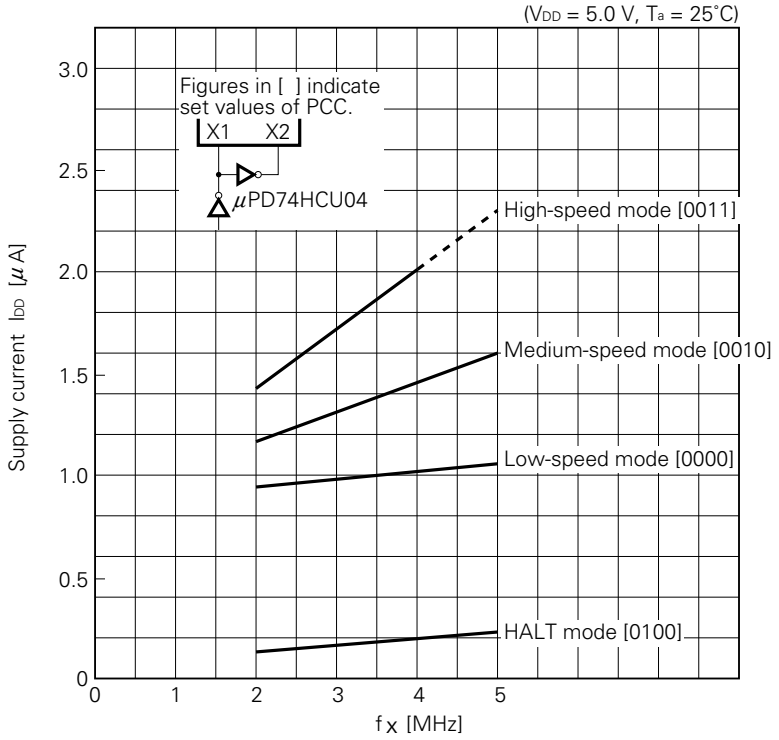
I_{DD} vs. V_{DD} Characteristics (ceramic oscillation)



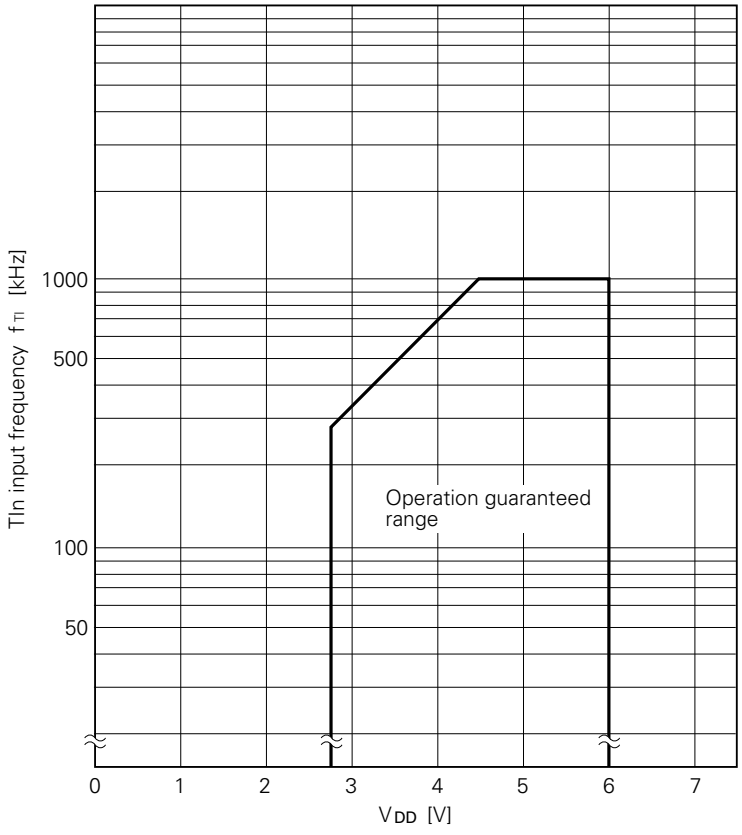
I_{DD} vs. f_{XX} Characteristics (ceramic oscillation)



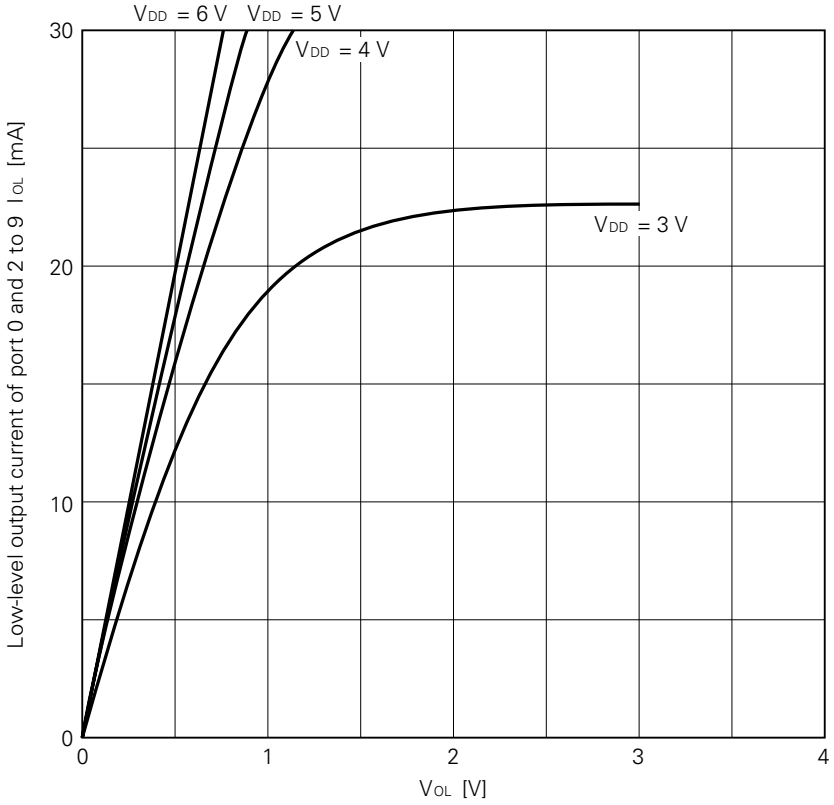
I_{DD} vs. f_X Characteristics (external clock)



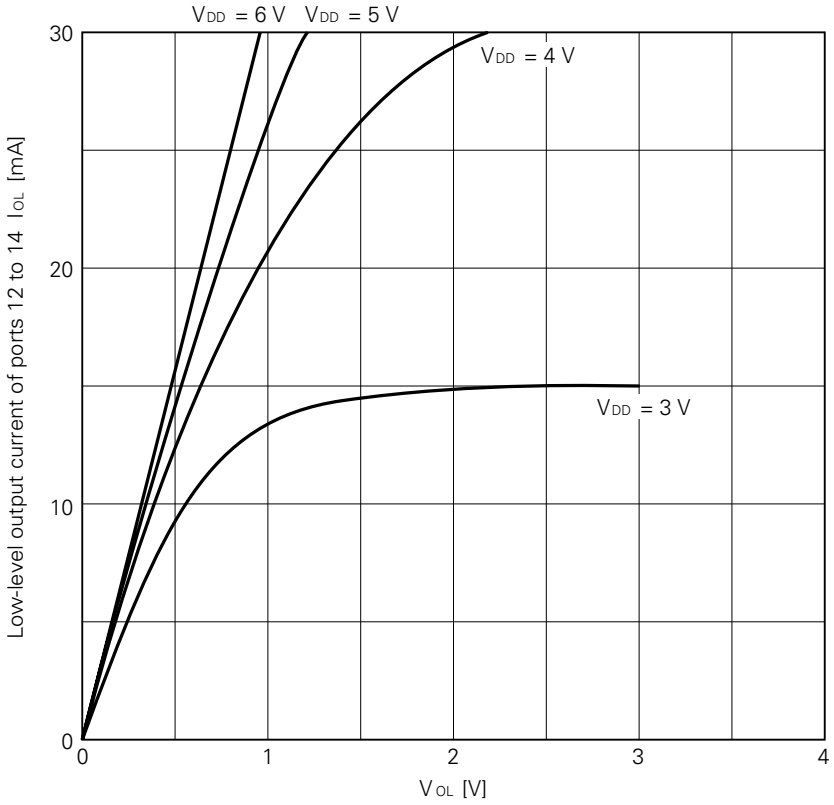
f_{TI} vs. V_{DD} Characteristics

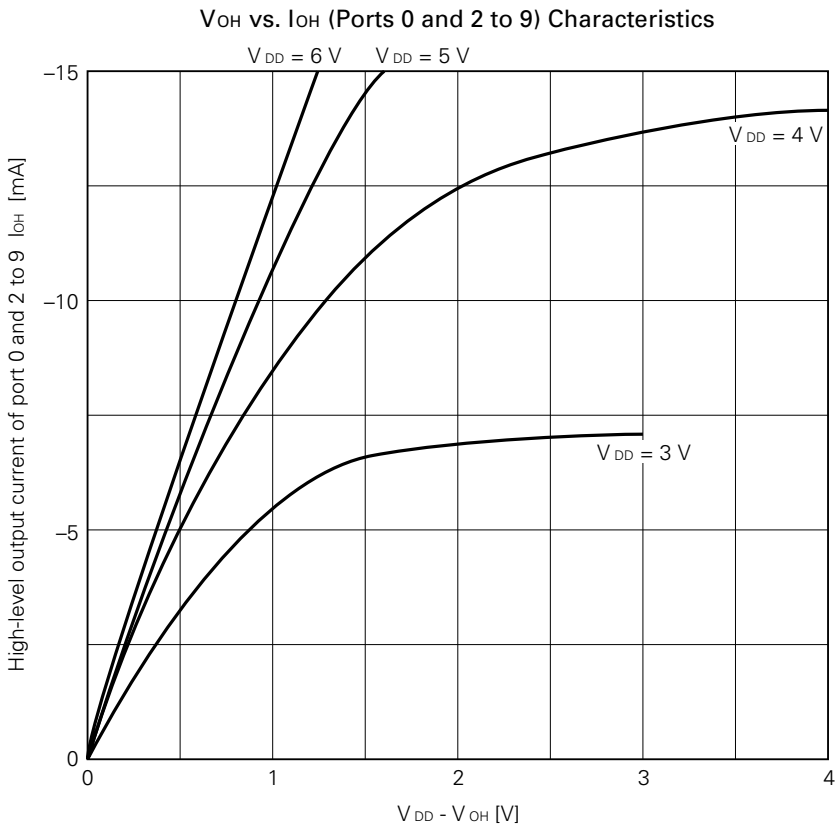


V_{OL} vs. I_{OL} (Ports 0 and 2 to 9) Characteristics



V_{OL} vs. I_{OL} (Ports 12 to 14) Characteristics

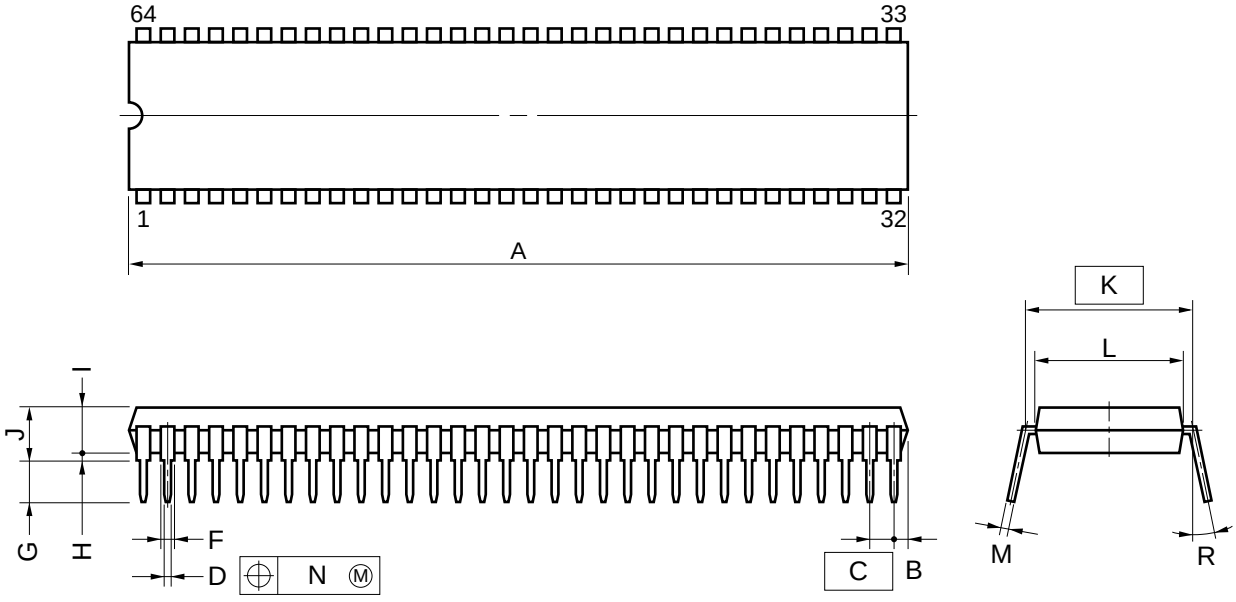




Remarks: Unless otherwise specified, all the characteristic data shown are reference values.

14. PACKAGE DRAWINGS

64 PIN PLASTIC SHRINK DIP (750 mil)



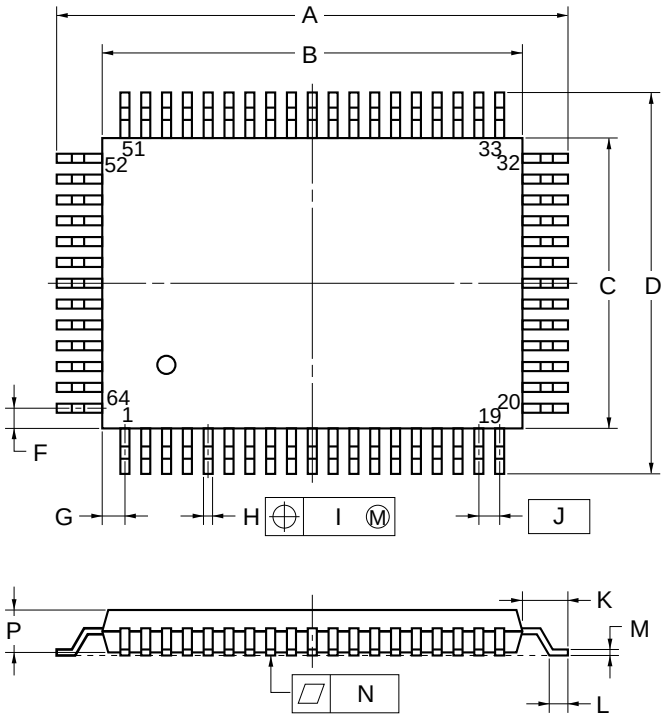
NOTE

1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.
2) Item "K" to center of leads when formed parallel.

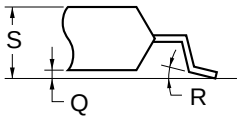
ITEM	MILLIMETERS	INCHES
A	58.68 MAX.	2.311 MAX.
B	1.78 MAX.	0.070 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	0.50 ± 0.10	$0.020^{+0.004}_{-0.005}$
F	0.9 MIN.	0.035 MIN.
G	3.2 ± 0.3	0.126 ± 0.012
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	19.05 (T.P.)	0.750 (T.P.)
L	17.0	0.669
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.17	0.007
R	0~15°	0~15°

P64C-70-750A,C-1

64 PIN PLASTIC QFP (14×20)



detail of lead end



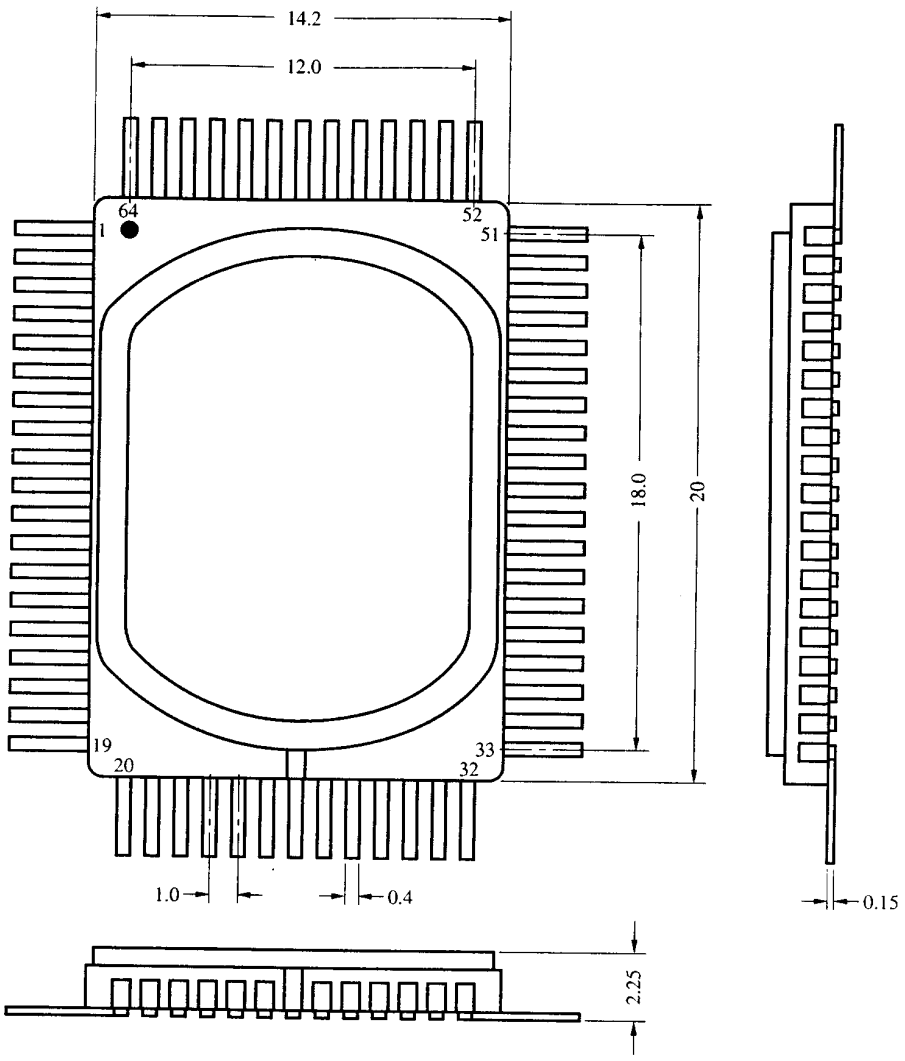
NOTE

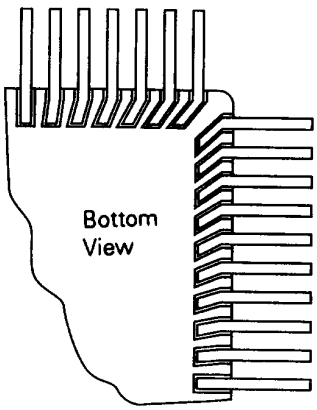
Each lead centerline is located within 0.20 mm (0.008 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	23.6±0.4	0.929±0.016
B	20.0±0.2	$0.795^{+0.008}_{-0.009}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.6±0.4	0.693±0.016
F	1.0	0.039
G	1.0	0.039
H	0.40±0.10	$0.016^{+0.004}_{-0.005}$
I	0.20	0.008
J	1.0 (T.P.)	0.039 (T.P)
K	1.8±0.2	$0.071^{+0.008}_{-0.009}$
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	2.7	0.106
Q	0.1±0.1	0.004±0.004
R	5°±5°	5°±5°
S	3.0 MAX.	0.119 MAX.

P64GF-100-3B8,3BE,3BR-2

ES 64-Pin Ceramic QFP (Reference) (unit in mm)





Note 1. The metal cap is connected to pin 26, at the Vss (GND) level.

2. The leads are molded diagonally at the bottom.
3. The lead lengths are not specified, as the lead cutting process is not controlled.

15. RECOMMENDED SOLDERING CONDITIONS

It is recommended that μPD75104, 75106, and 75108 be soldered under the following conditions.

For details on the recommended soldering conditions, refer to Information Document "Semiconductor Devices Mounting Manual" (IEI-616).

For other soldering methods and conditions, please consult NEC.

Table 15-1 Soldering Conditions of Surface Mount Type

μPD75108GF - xxx - 3BE: 64-pin plastic QFP (14 x 20 mm)

Soldering Method	Soldering Conditions	Symbol for Recommended Condition
Infrared Reflow	Package peak temperature: 230°C, time: 30 seconds max. (210°C min.), number of times: 1	IR30-00-1
VPS	Package peak temperature: 215°C, time: 40 seconds max. (200°C min.), number of times: 1	VP15-00-1
Wave Soldering	Soldering bath temperature: 260°C max., time: 10 seconds max., number of times: 1, pre-heating temperature: 120°C max. (package surface temperature)	WS60-00-1
Pin Partial Heating	Pin temperature: 300°C max., time: 3 seconds max. (per side)	—

Caution: Do not use two or more soldering methods in combination (except the pin partial heating method).

Table 15-2 Soldering Conditions of Through-Hole Type

μPD75108CW - xxx : 64-pin plastic shrink DIP (750 mil)

Soldering Method	Soldering Conditions
Wave Soldering (Only for lead part)	Soldering bath temperature: 260°C max., Time: 10 seconds max.
Pin Partial Heating	Pin temperature: 260°C max., Time: 10 seconds max.

Caution: The wave soldering must be performed at the lead part only. Note that the solder must not be directly contacted to the package body.

APPENDIX A. FUNCTIONAL DIFFERENCES AMONG PRODUCTS IN μPD751XX SERIES

Item		μPD75104	μPD75106	μPD75108	μPD75112	μPD75116	μPD75104A	μPD75108A	μPD75108F	μPD75112F	μPD75116F	μPD75P108B	μPD75P116
ROM Configuration		Mask ROM										PROM	
ROM (Bits)		000H-FFFH 4096 × 8	0000H-177FH 6016 × 8	0000H-1F7FH 8064 × 8	0000H-2F7FH 12160 × 8	0000H-3F7FH 16256 × 8	000H-FFFH 4096 × 8	0000H-1F7FH 8064 × 8	0000H-1F7FH 8064 × 8	0000H-2F7FH 12160 × 8	0000H-3F7FH 16256 × 8	0000H-1F7FH 8064 × 8	0000H-3F7FH 16256 × 8
RAM (Bits)		320 × 4 (Bank 0: 256 × 4) (Bank 1: 64 × 4)		512 × 4 (Bank 0: 256 × 4) (Bank 1: 256 × 4)			320 × 4 (Bank 0: 256 × 4) (Bank 1: 64 × 4)	512 × 4 (Bank 0: 256 × 4) (Bank 1: 256 × 4)	512 × 4 (Bank 0: 256 × 4) (Bank 1: 256 × 4)				
Instruction Set		High-end (Only μPD75104 and 75104A are not provided with BR!addr instruction.)							High end				
I/O Lines	Total	58											
	I/O	• CMOS I/O: 32 • +12 V open-drain output: 12 (pull-up resistor as mask option) LED direct drive: 44					• CMOS I/O: 32 (pull-up resistor as mask option: 24) • +12 V open-drain output: 12 (pull-up resistor as mask option) LED direct drive: 44		• CMOS I/O: 32 • +10 V open-drain output: 12 (pull-up resistor as mask option) LED direct drive: 44			• CMOS I/O: 32 • +12 V open-drain output: 12 LED direct drive: 44	
	Input	• CMOS input: 10 • Comparator input: 4					• CMOS input: 10 (pull-up resistor as mask option: 4) • Comparator input: 44		• CMOS input: 10 • Comparator input: 4				
Power-ON Reset Circuit		Provided (mask option)							None				
Power-ON Flag													
Operating Voltage Range		2.7 to 6.0 V							2.7 to 5.0 V (T_a = -40 to +50°C) 2.8 to 5.0 V (T_a = -40 to +60°C)			2.7 to 6.0 V	5 V ± 10%
Minimum Instruction Execution Time		0.95 μs (at 5 V) 3 μs (at 3 V)							0.95 μs (at 4.5 V to 5.0 V) 1.91 μs (at 3 V)			0.95 μs (at 5 V) 3 μs (at 3 V)	0.95 μs (at 5 V)
Pin Connections		Depends on package							Depends on package. Only μPD75P108, and 75P116 are provided with V_{PP} pin.				
Package		• 64-pin plastic shrink DIP (750 mil) • 64-pin plastic QFP (14 × 20 mm)			• 64-pin plastic shrink DIP (750 mil) • 64-pin plastic QFP (14 × 20 mm)		• 64-pin plastic QFP (14 × 14 mm)	• 64-pin plastic QFP (14 × 14 mm) • 64-pin plastic QFP (14 × 14 mm)	• 64-pin plastic QFP (14 × 20 mm)			• 64-pin plastic shrink DIP (750 mil) • 64-pin ceramic shrink DIP (w/window) • 64-pin plastic QFP (14 × 20 mm)	• 64-pin plastic shrink DIP (750 mil) • 64-pin plastic QFP (14 × 20 mm)

APPENDIX B. DEVELOPMENT TOOLS

The following development support tools are readily available to support development of systems using μPD75108:

Hardware	IE-75000-R*1 IE-75001-R	In-circuit emulator for 75X series
	IE-75000-R-EM*2	Emulation board for IE-75000-R and IE-75001-R
	EP-75108CW-R	Emulation prove for μPD75108CW
	EP-75108GF-R EV-9200G-64	Emulation prove for μPD75108GF. It is provided with a 64-pin conversion socket, EV-9200G-64
	PG-1500	PROM programmer
	PA-75P108CW	PROM programmer adapter for μPD75P108BCW and 75P108BDW. It is connected to PG-1500.
	PA-75P116GF	Programmer adapter for μPD75P108BGF. It is connected to PG-1500.
Software	IE Control Program	Host machine PC-9800 series (MS-DOS™ Ver.3.30 to Ver.5.00A*3) IBM PC/AT™ (PC DOS™ Ver.3.1)
	PG-1500 Controller	
	RA75X Relocatable Assembler	

*1: Maintenance product

2: Not provided with IE-75001-R.

3: Ver.5.00/5.00A has a task swap function, but this function cannot be used with this function.

Remarks: For development tools from other companies, refer to 75X Series Selection Guide (IF-151).

APPENDIX C. RELATED DOCUMENTS

GENERAL NOTES ON CMOS DEVICES

① STATIC ELECTRICITY (ALL MOS DEVICES)

Exercise care so that MOS devices are not adversely influenced by static electricity while being handled.

The insulation of the gates of the MOS device may be destroyed by a strong static charge. Therefore, when transporting or storing the MOS device, use a conductive tray, magazine case, or conductive buffer materials, or the metal case NEC uses for packaging and shipment, and use grounding when assembling the MOS device system. Do not leave the MOS device on a plastic plate and do not touch the pins of the device.

Handle boards on which MOS devices are mounted similarly .

② PROCESSING OF UNUSED PINS (CMOS DEVICES ONLY)

Fix the input level of CMOS devices.

Unlike bipolar or NMOS devices, if a CMOS device is operated with nothing connected to its input pin, intermediate level input may be generated due to noise, and an inrush current may flow through the device, causing the device to malfunction. Therefore, fix the input level of the device by using a pull-down or pull-up resistor. If there is a possibility that an unused pin serves as an output pin (whose timing is not specified), each pin should be connected to V_{DD} or GND through a resistor.

Refer to "Processing of Unused Pins" in the documents of each devices.

③ STATUS BEFORE INITIALIZATION (ALL MOS DEVICES)

The initial status of MOS devices is undefined upon power application.

Since the characteristics of an MOS device are determined by the quantity of injection at the molecular level, the initial status of the device is not controlled during the production process. The output status of pins, I/O setting, and register contents upon power application are not guaranteed. However, the items defined for reset operation and mode setting are subject to guarantee after the respective operations have been executed.

When using a device with a reset function, be sure to reset the device after power application.

[MEMO]

M4 92.6