TOSHIBA INTEGRATED CIRCUIT

TECHNICAL DATA

TD6301AP, TD6301AN

TOSHIBA I^2L DIGITAL INTEGRATED CIRCUIT

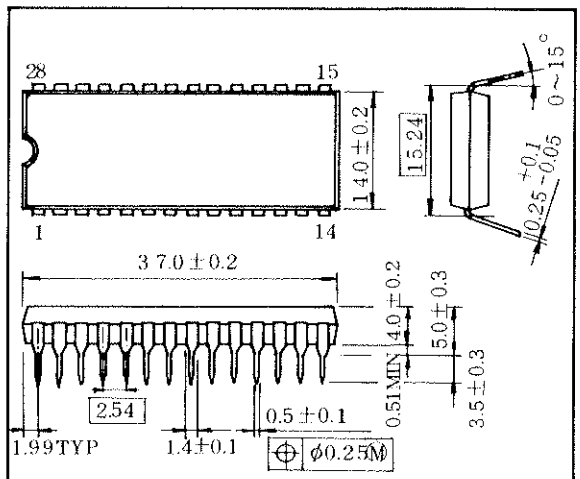
SILICON MONOLITHIC

STATIC DRIVER FOR LED/LCD RECEIVING FREQUENCY DISPLAY

TD6301AP/AN is a static driver for a receiving frequency digital display developed for TOSHIBA digital tuning system, DTS-6 and DTS-8.
This unit latches serial data transferred in one cycle only at time of station selecting operation from the system controller, and statically displays the data by performing compensation operation of intermediate frequency.
Since the output circuit contains a driver, no external transistors are required.

- Operating voltage : 5V±0.5V
- Display of static system affords improvement in S/N and simplification of set design.
- Output circuit has a built-in transistors for large current flow as well as high resisting voltage; therefore, this unit can be used for all of LED, FL(fluorescent lamp), LCD(liquidcrystal display), requiring no external transistors.
- Number of display digits is a 3 digits and a half up to 1999 at maximum, and the digits of FM 50kHz are driven by system controller.
- Data transfer from the system controller can be made through connection of three wires because of a serial system.
- TC9137BP, TC9147BP, TC9157AP can be also used in combination with this TD6301AP/AN.

Unit in mm

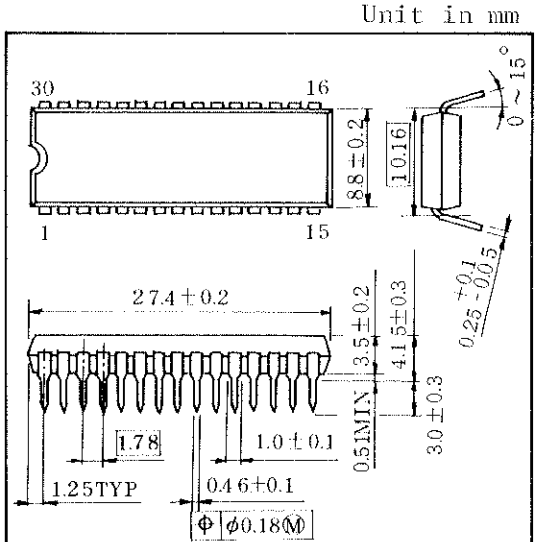


Package width and length do not include mold protrusion.
Allowable mold protrusion is 0.15mm.

JEDEC	—
TOSHIBA	DIP28-P-600

Weight : 4.4g

Unit in mm



Package width and length do not include mold protrusion.
Allowable mold protrusion is 0.15 mm.

JEDEC	—
TOSHIBA	SDIP30-P-400

Weight : 2.2g

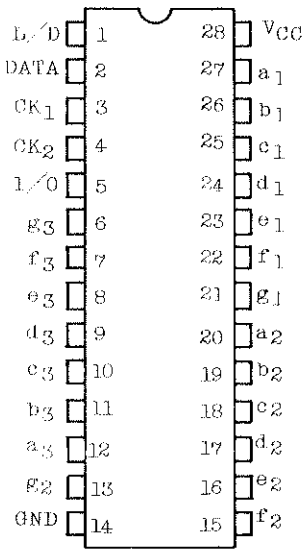
MAXIMUM RATINGS (Ta=25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{CC}	8	V
Input Voltage	V_{IN}	-0.3~V_{CC}+0.3	V
Output Current	$I_{OL(MAX)}$	20	mA
Output Voltage	$V_{OH(MAX)}$	20	V
Power Dissipation	P_D	1.0(0.8)	W
Operating Temperature	T_{opr}	-30~75	°C
Storage Temperature	T_{stg}	-55~150	°C

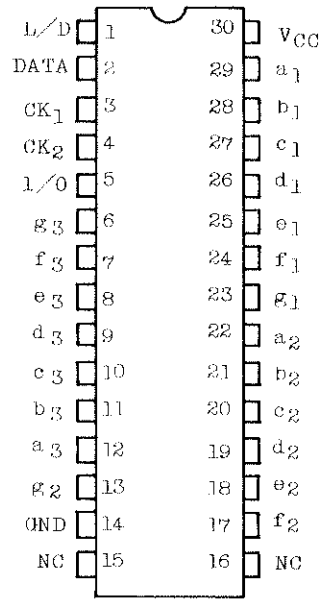
( ) : TD6301AN

PIN CONNECTIONS

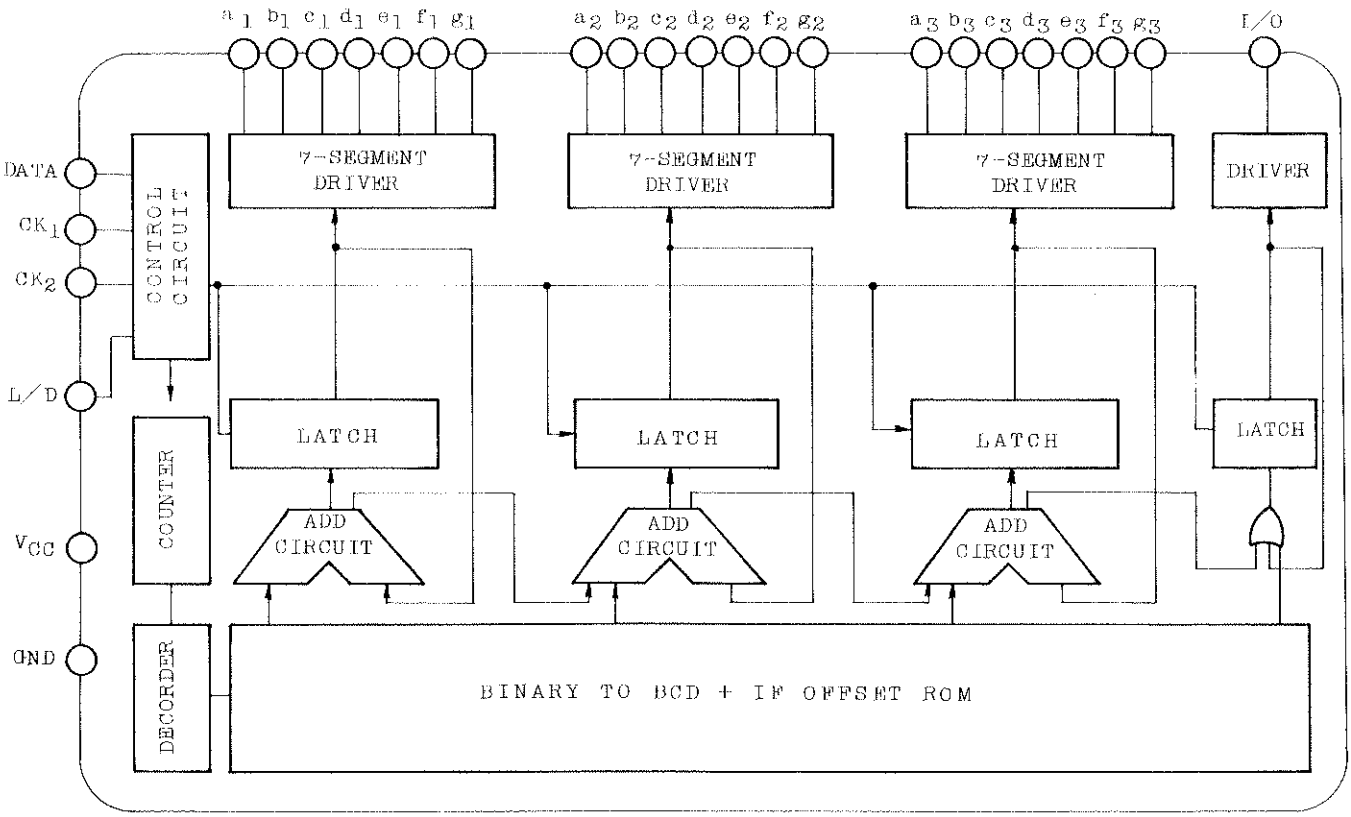
TD6301AP



TD6301AN



BLOCK DIAGRAM



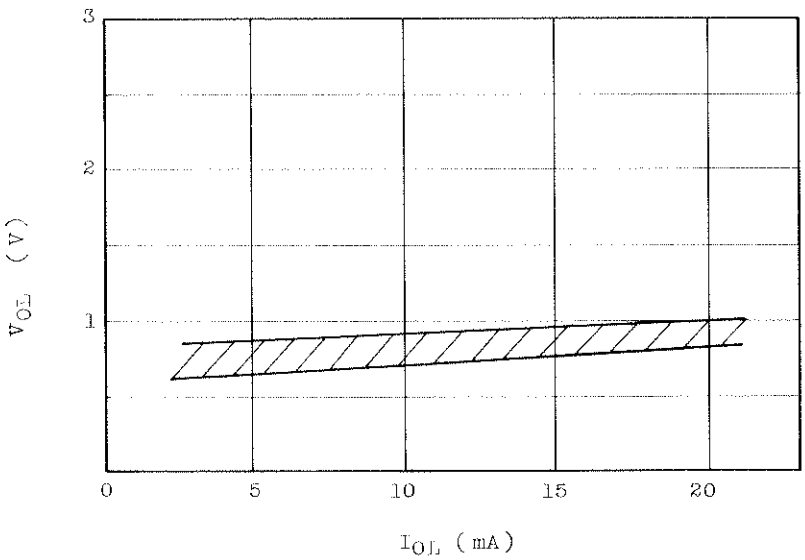
PIN DESCRIPTION (Data in parenthesis are for TD6301AN)

PIN No.	NAME	FUNCTIONAL DESCRIPTION	REMARKS
1 (1)	L/D	Output state switching signal input. Signal input for switching output state by displays (LED, FL and LCD).	
2 (2)	Data	Receiving frequency data signal input. Signal is input in serial from system controller.	
3,4 (3,4)	CK_1,CK_2	Timing clock signal input.	
5 (5)	I/O	Segment drive signal output. For FM the digit of 100MHz and for AM that of 1000kHz are displayed respectively. Since both FM and AM are 1 or 0, one pin only is sufficient for output.	With built-in transistors of high resisting voltage and large current flow.
6~12 (6~12)	a_3~g_3	7-segment drive signal output. Digits of 10MHz for FM and those of 100kHz for AM are displayed, respectively.	"
13,15~20 (13,17~22)	a_2~g_2	7-segment drive signal output. Digits of 1MHz for FM and those of 10kHz for AM and displayed, respectively.	"
21~27 (23~29)	a_1~g_1	7-segment drive signal output. Digits of 100kHz for AM and those of 1kHz for AM are displayed, respectively.	"
14,28 (14,30)	V_{CC},GND	Power supply and GND.	
(15,16)	NC	No connection (TD6301AN only)	

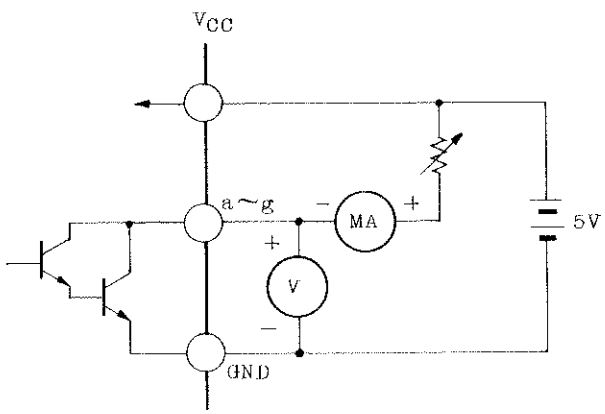
ELECTRICAL CHARACTERISTICS (Unless otherwise specified, V_{CC}=5V, Ta=25°C)

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Supply Voltage Range		V_{CC}	-	Ta=-30~75°C	4.5	5.0	5.5	V
Operating Supply Current		I_{CC}	-	No load	-	-	16	mA
Input Voltage	"H" Level	V_{IH}	-	Data, CK_1, CK_2, L/D	4.0	-	-	V
	"L" Level	V_{IL}	-	"	-	-	1.0	V
Input Current	"H" Level	I_{IH}	-	" V_{IH}=5V	-	-	0.6	mA
	"L" Level	I_{IL}	-	" V_{IL}=0V	-0.1	-	-	mA
Output Current		I_O	1	a_1~g_1, a_2~g_2, a_3~g_3, 1/0	15	-	-	mA
Output Saturation Voltage		$V_{CE(sat)}$	1	" I_{OL}=15mA	-	-	1.2	V
Timing Input Operating Frequency		fopr	-	Data, CK_1, CK2	-	-	120	kHz

V_{OL} - I_{OL}



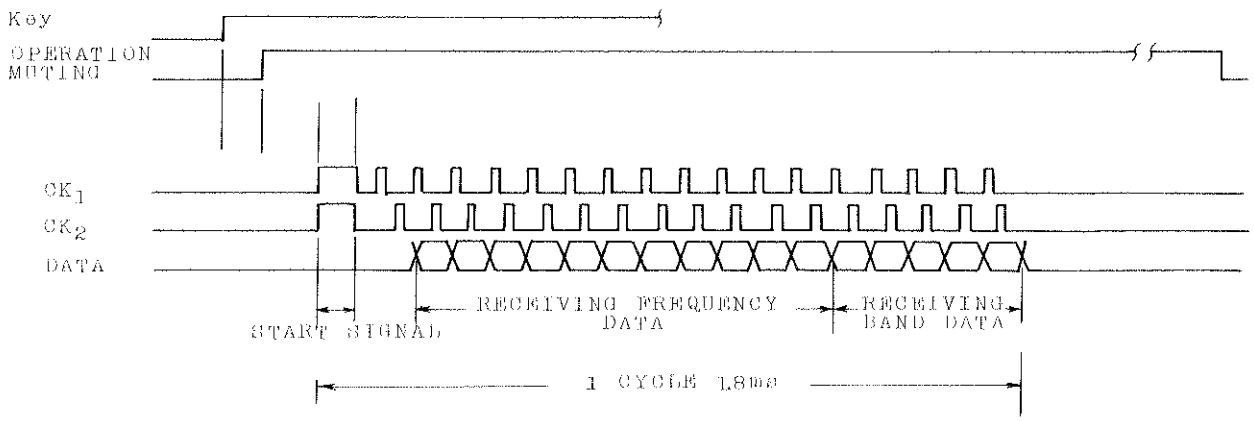
TEST CIRCUIT (1)



OPERATIONAL DESCRIPTION

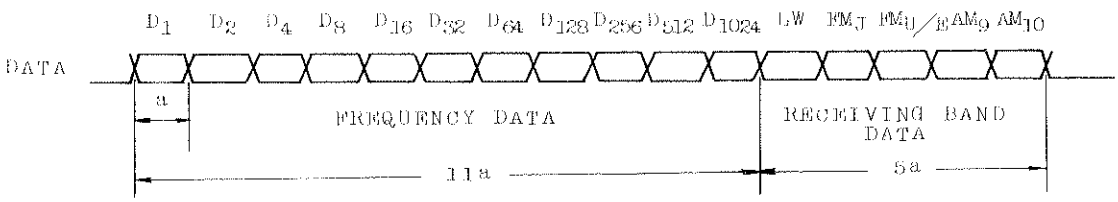
1. RECEIVING FREQUENCY DATA

Only when a receiving frequency is updated with the system power ON, up/down operation, automatic scanning, memory calling, FM/AM switching, etc., the following timing signals and serial data signals are transferred in one cycle only from system controller.



1-1) Data signal (Data)

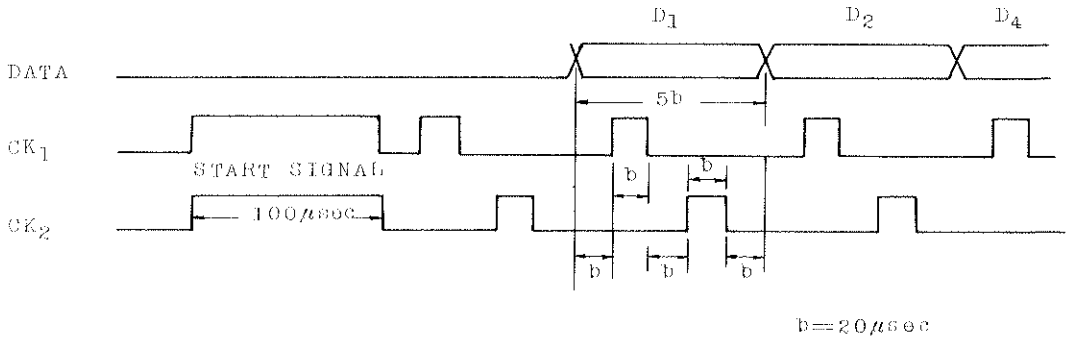
The data signal consists of 16 bits; their 11 bits are designed to frequency data signal and their 5 bits to receiving band ($LW/FM_J/FM_U/AM_9/AM_{10}$) signal.



$a = 100\mu sec$

1-2) Timing signals (CK_1, CK_2)

This driver is provided with two lines of CK_1 and CK_2 for read-in timing of data signal, permitting the following timing between data signal and each timing signal.



1-3) Frequency data

The frequency data consists of 11 bits, being transferred in binary code from system controller.
Each data for $AM_9/AM_{10}/FM_L/FM_U/E/LW$.

o AM_9 (Japan, Europe)

522kHz	531kHz	540kHz	549kHz	---------- 1602kHz	1611kHz
0	9	18	27	---------- 1080	1089

o AM_{10} (U.S.A.)

520kHz	530kHz	540kHz	550kHz	---------- 1600kHz	1610kHz
0	10	20	30	---------- 1080	1090

o FM_L (Japan)

76.0	76.1	76.2MHz	---------- 89.9MHz	90.0MHz
0	1	2	---------- 139	140

o FM_U (U.S.A.)

87.5	87.6	87.7MHz	---------- 107.9MHz	108.0MHz
0	1	2	---------- 204	205

o FM (Europe)

87.50	87.55	87.60	87.65MHz	----------	107.95	108.00MHz
0	0	1	1	----------	205	205

o LW (Europe)

153	154	155kHz	----------	359	360kHz
0	1	2	----------	206	207

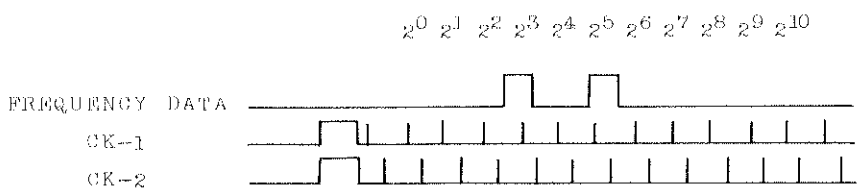
o The upper row shows the receiving frequencies of respective bands.

The lower row shows the frequency data at each time.

AM_9 (Receiving frequency) - 522
AM_{10} (") - 520
FM_J (") - 760
FM_U (") - 875
FM_E (") - 875
LW (") - 153

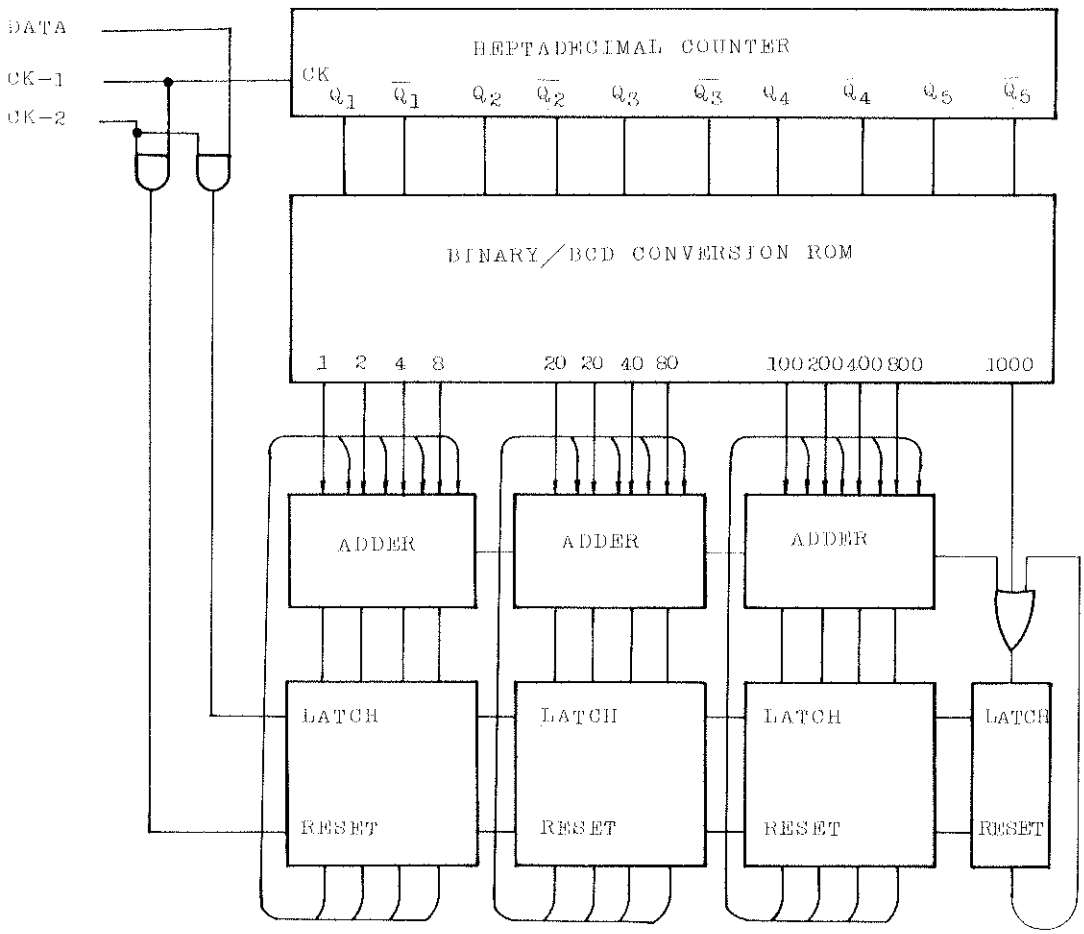
o At time of FM, the data are taken as no decimal and for FM_E the digit of 50 kHz is neglected.

(Example) The data at time of Japanese band FM 800MHz becomes 800 - 760 = 40, and the then data output is follows:



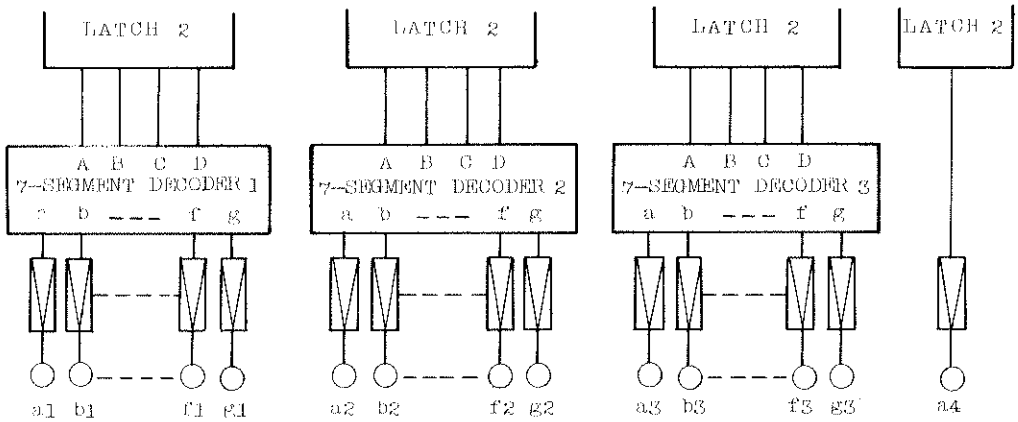
2. DATA CONVERSION

Since the frequency data are binary code and serial input, they must be converted into BCD code parallel. TD6301AP/AN converts the frequency data transferred from the system controller by two timing signals of CK1 and CK2.



3. SEGMENT DRIVER

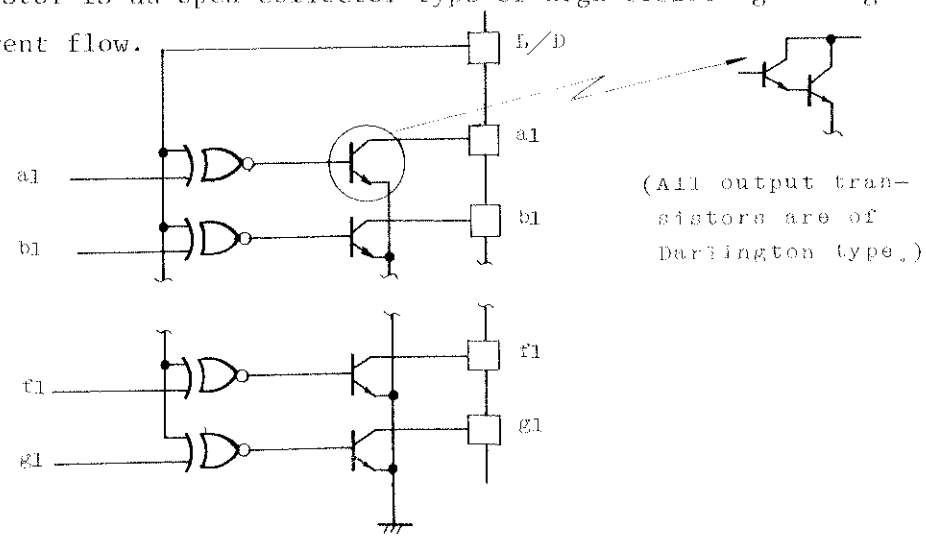
The segment driver decodes the 4-digit BCD code latched to the latch$_2$ with every digit by a segment decoder, and outputs the data.



Since the high-order position is nothing but 1 on data, it is output by "1" or "0".

4. OUTPUT CIRCUIT

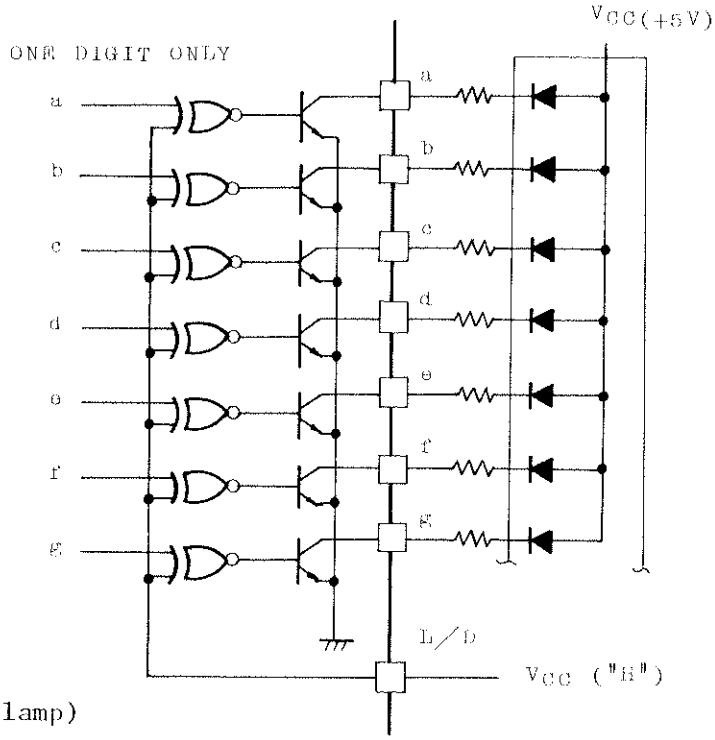
The output circuit is considered to be used for all of LED, FL (fluorescent lamp), and LCD (liquid-crystal display). The output circuit is used for various displays in L/D terminal state.
The transistor is an open collector type of high resisting voltage and large current flow.



5. APPLICATIONS BY DISPLAYS

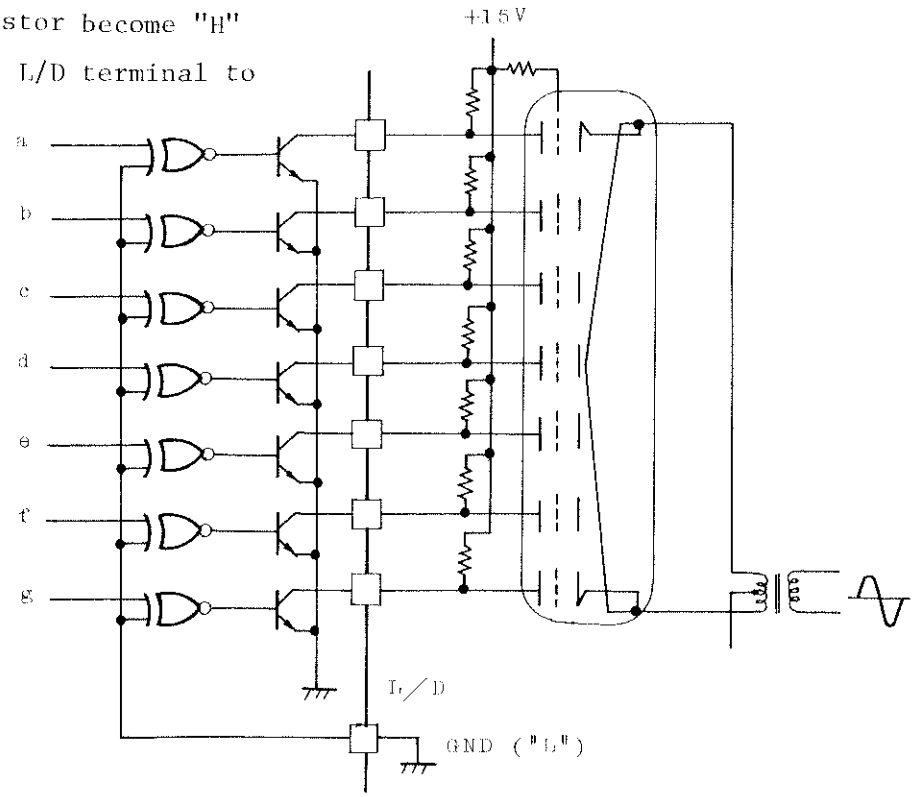
5-1) LED

The output transistors become "L" active by setting L/D terminal to "H" level.



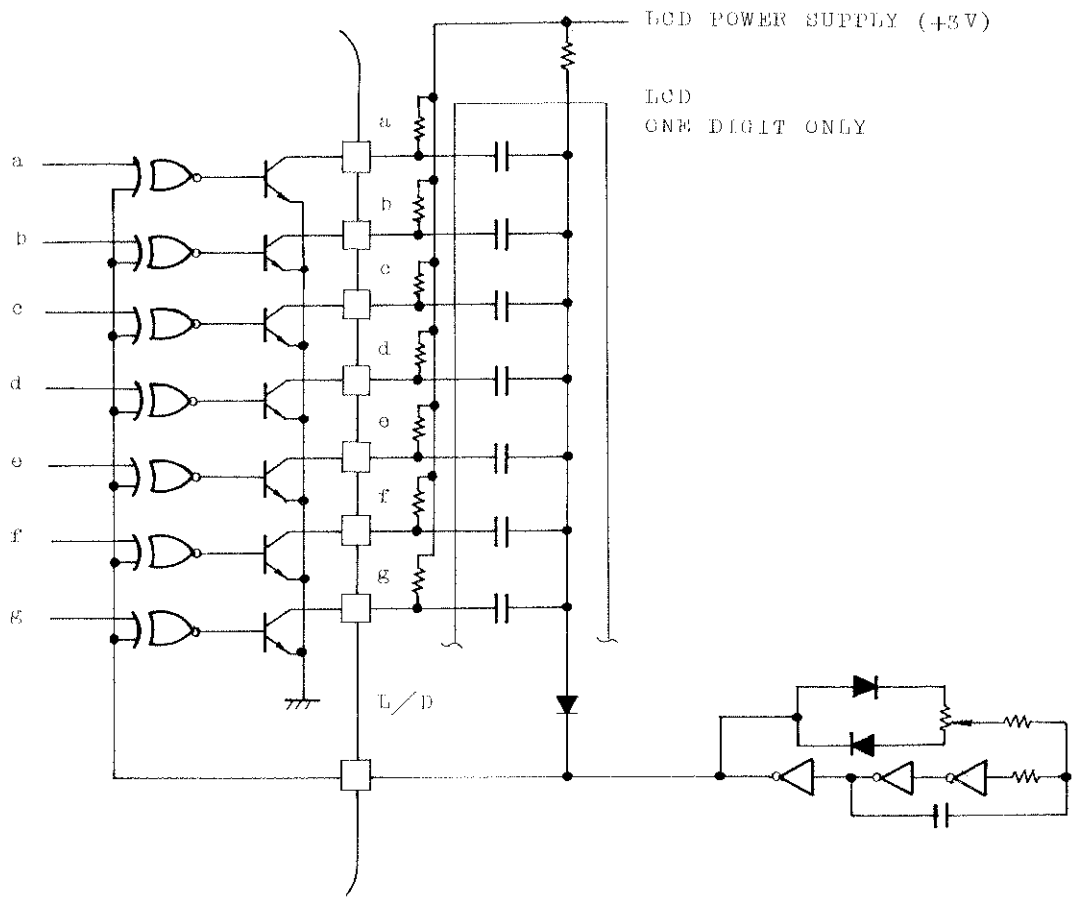
5-2) FL (Fluorescent lamp)

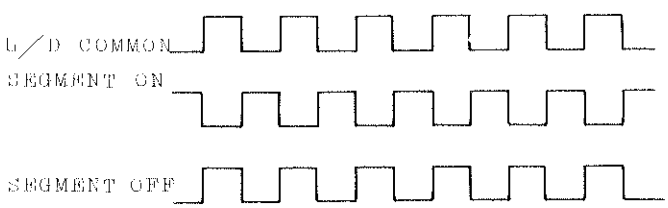
The output transistor become "H" active by setting L/D terminal to "L" level.



5-3) LCD (Liquid-crystal display)

TD6301AP/AN is also designed to drive LCD.





Since LCD is AC driven, the input is fed into the LCD common through L/D after the oscillator of the required frequency has been externally made.

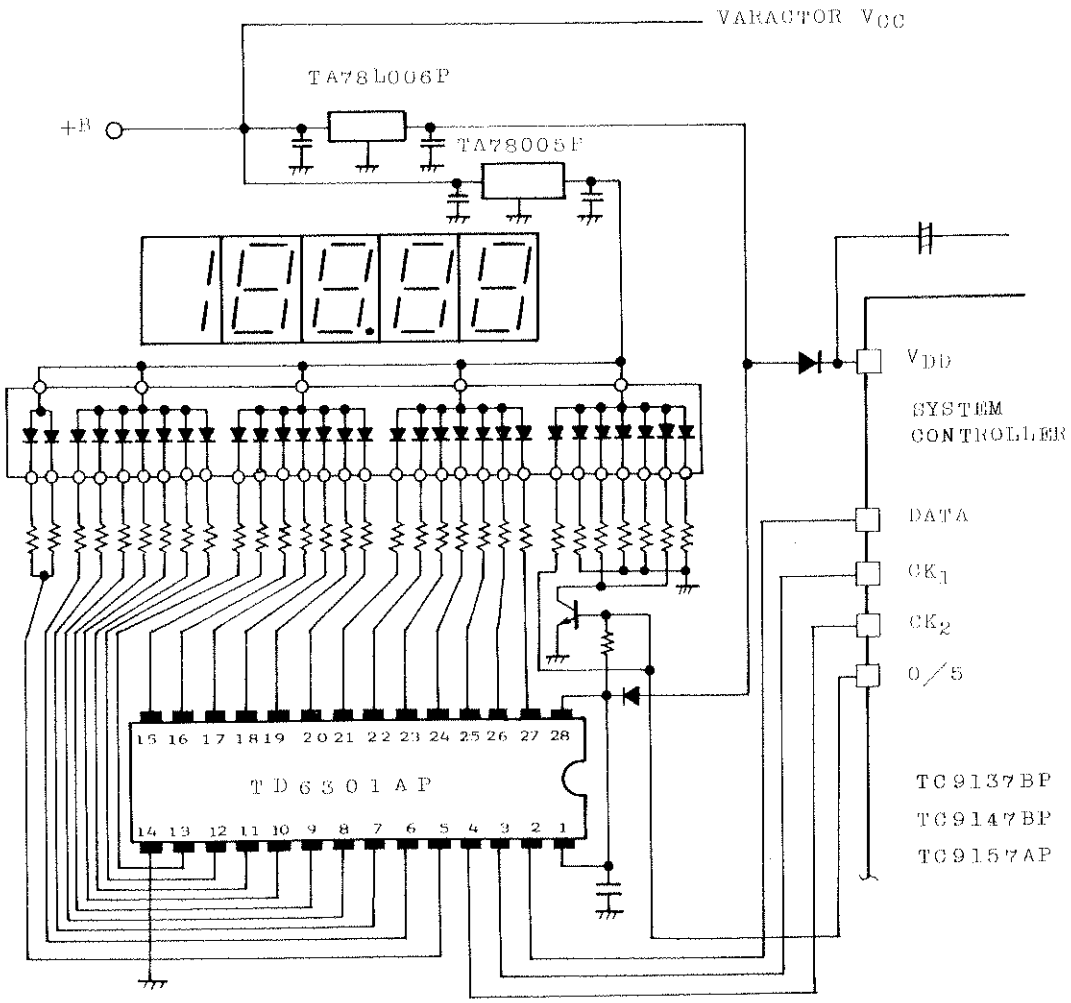
With the segment "ON", the L/D terminal and segment decoder output is (becomes) Exclusive OR; therefore, the phase between the common and the segment becomes anti-phase and the LCD is lighted.
On the contrary, with the segment "OFF" the phase between common and the segment becomes same-phase and the LCD is not lighted.

6. FONT OF DISPLAY

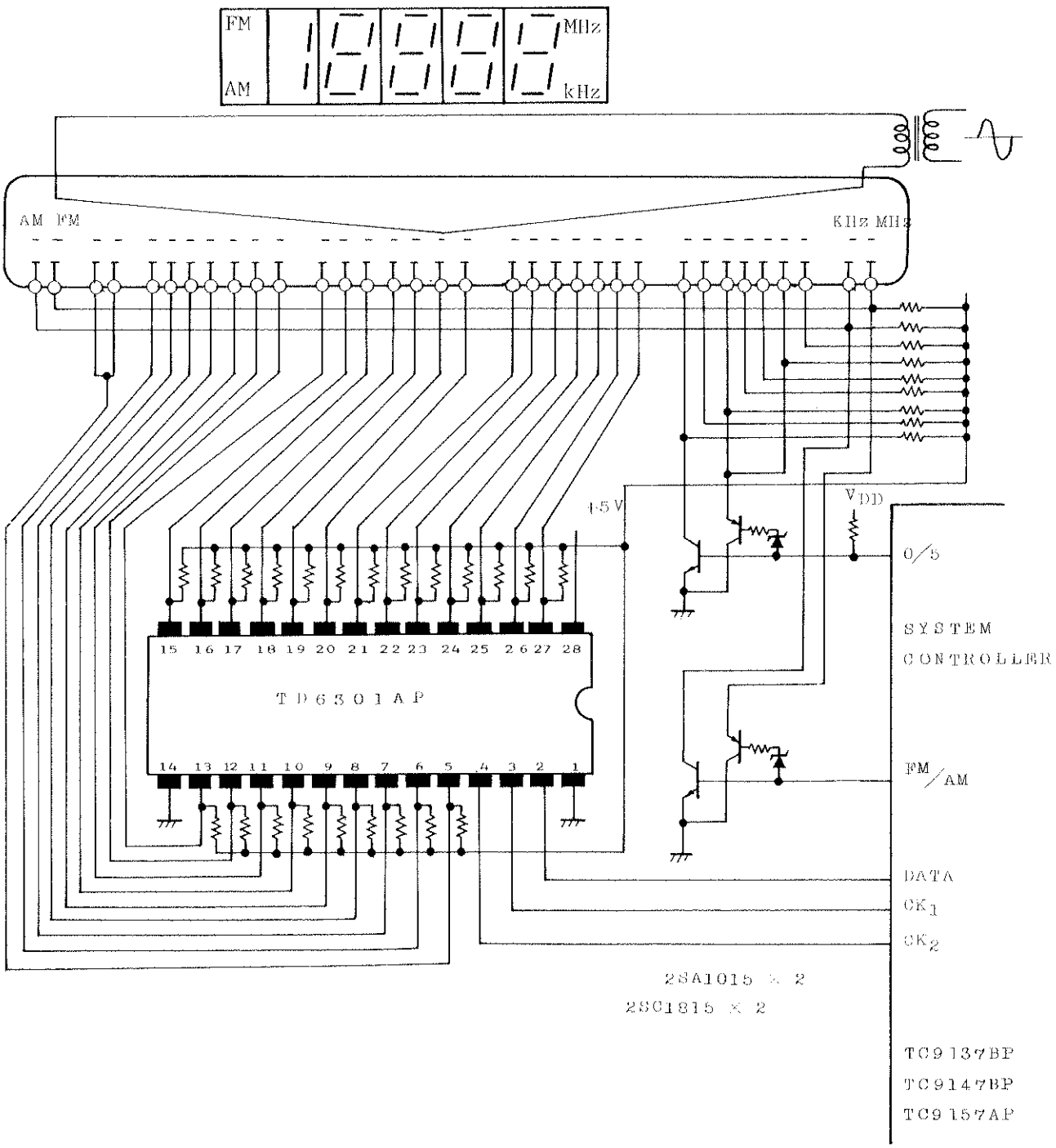
The display of TD6301AP/AN becomes the font shown below.

7. EXAMPLES OF APPLIED CIRCUIT

EXAMPLE OF LED DRIVE



EXAMPLE OF FL DRIVE



EXAMPLE OF LCD DRIVE

(Including FM, AM, MHz, and kHz display.)