February 1990
Edition 5.0

FUJITSU

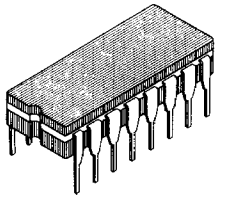
DATA SHEET

MB4052
4-CHANNEL 8-BIT A/D CONVERTER

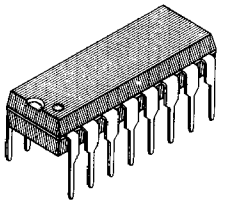
4-CHANNEL 8-BIT A/D CONVERTER SUBSYSTEM

The Fujitsu MB 4052 is an analog-to-digital converter (ADC) for general purpose which features four channels of analog inputs and 8-bit data length of digital output.
Analog input signal is converted to serial 8-bit digital data by the successive-approximation technique which provides high-speed conversion, i.e. many analog data can be converted within a short time.
All digital I/O signals including control inputs are TTL level compatible so as to provide wide application such as in microprocessor-controlled system and so on.

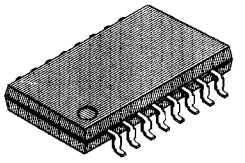
- Single Power Supply;
  DIP: +3.5V to +6.0V or +8.0V to +18V (with Internal Regulator)
  FPT: +3.5V to +6.0V or +8.0V to +13.2V (with Internal Regulator)
- Multiplex 4-Channel Analog Inputs
- Changeable Analog Input Voltage Ranges:
  0 to 2.5V (Standard mode: RS = 1)
  0 to 0.625V (Contracted mode: RS = 0)
  0 to 10V (Expanded mode: through built-in Divider)
- Analog Input Bias Current: 250nA Max.
- Resolution: 8 bits
- Linearity: 0.19% Max.
- Successive-Approximation Conversion: 100μs/ch Max. at f_{CLK} = 100 kHz
- Ratio-Metric Conversion by Reference Voltage V_{CC1}
- Serial Data Output (Open-Collector)
- TTL/CMOS Compatible Digital I/O
- Package: DIP-16C-C02
  DIP-16P-M04
  FPT-16P-M03



CERAMIC PACKAGE
DIP-16C-C02

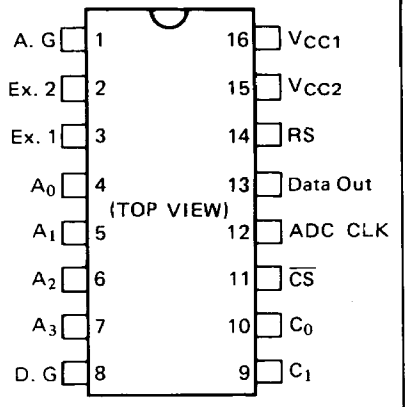


PLASTIC PACKAGE
DIP-16P-M04



PLASTIC PACKAGE
FPT-16P-M03

PIN ASSIGNMENT



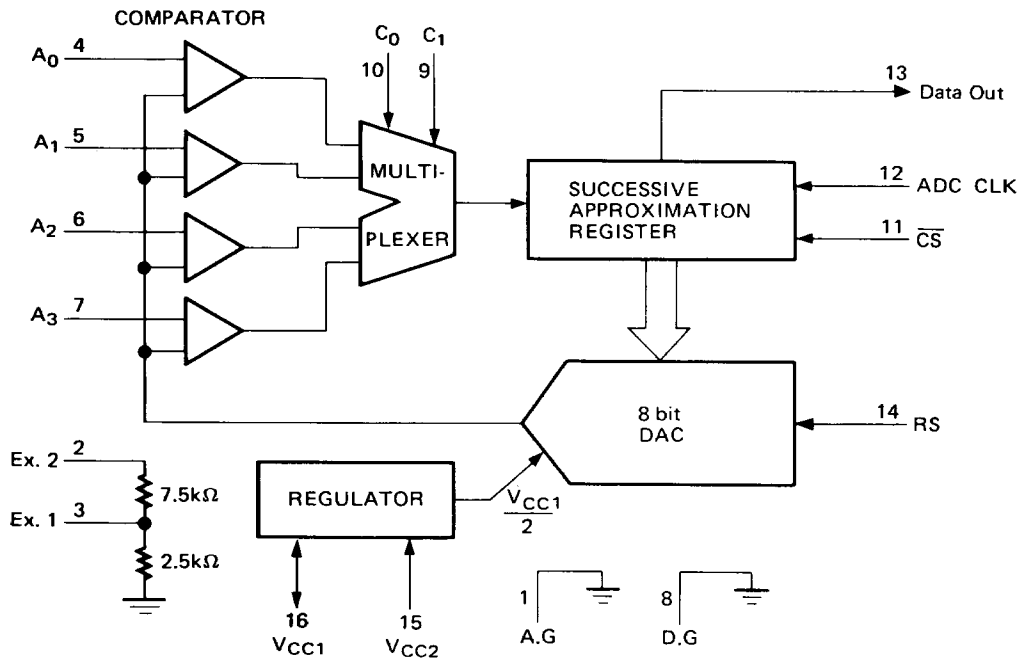
ABSOLUTE MAXIMUM RATINGS (All Voltages referenced to A.G/D.G)

Rating		Symbol	Value	Unit
Power Supply Voltage		V_{CC1}	+7	V
		V_{CC2}	+20	V
Digital Input Voltage		V_{ID}	−0.5 to +20	V
Digital Output Voltage (Off-State)		V_{OH}	+20	V
Analog Input Voltage		V_{IA}	V_{CC1}+0.5	V
Storage Temperature	Ceramic	T_{STG}	−55 to +150	°C
	Plastic		−40 to +125	

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1— MB 4052 BLOCK DIAGRAM



RECOMMENDED OPERATING CONDITIONS

(T_A = -30°C to +85°C)

Parameter	Symbol		Value			Unit
			Min.	Typ.	Max.	
Power Supply Voltage	V_{CC1}		3.5	5.0	6.0	V
	V_{CC2}	DIP	8.0	12.0	18.0	V
		FPT	8.0	12.0	13.2	V
Digital Output Low Current	I_{OL}		–	–	8	mA
Operating Temperature	T_A		-30	–	+85	°C

PIN DESCRIPTIONS

INPUT FOR VOLTAGE RANGE EXPANSION (EX 2), PIN 2

This input pin is provided to expand the voltage range of analog input signal.
This input pin is connected to the internal one-to-four voltage divider which reduces an analog signal level to one fourth of input level.

OUTPUT FOR VOLTAGE RANGE EXPANSION (EX 1), PIN 3

This output pin is provided to expand the allowable analog input level in co-operation with the above EX 2 pin.
A reduced signal which is divided in the internal divider is output on this pin.
This output pin can be connected to any of standard analog inputs A_0, A_1, A_2 or A_3 so that the EX 2 pin can function as one of 4-channel inputs.

ANALOG INPUTS (A_0 TO A_3), PINS 4, 5, 6 AND 7

These input pins are provided to receive four channels of analog inputs.
One of these four channels is selected by a combination of C_0 and C_1 inputs.

CHANNEL SELECT (C_1 AND C_0), PINS 9 AND 10

These control inputs are used to designate one of four analog inputs as shown in Table 1.

Table 1 CHANNEL SELECTION

C_1	C_0	Channel
0	0	A_0
0	1	A_1
1	0	A_2
1	1	A_3

CHIP SELECT ($\overline{CS}$), PIN 11

This control input pin is used to start analog-to-digital conversion.
When $\overline{CS}$ goes low, the A/D conversion start and the DATA OUT output is enabled.
When an A/D conversion is completed or termination of conversion is required, $\overline{CS}$ is made high.

A/D CONVERSION CLOCK (ADC CLK), PIN 12

This clock signal is input to the internal successive approximation register and used as timing signal for A/D conversion.
The conversion speed of this device is determined by this clock rate.
Ten clock cycles are required for a complete 8-bit conversion.
A precise cycle time is not always required for this clock signal.

DATA OUTPUT (DATA OUT), PIN 13

This output pin is provided to output the A/D conversion results as digital signals.
The converted digital data are serially output in the order of start-bit, MSB (Most Significant Bit), 2SB (Second Significant Bit), ... , 7SB, LSB (Least Significant Bit) and stop-bit in synchronization with the ADC CLK clock signal.

RANGE SELECT (RS), PIN 14

This control input is provided to select an analog input voltage range as shown in Table 2.
This input must not be changed during an A/D conversion.

Table 2 RANGE SELECTION

RS	Voltage Range
0	0 to 1/8 V_{CC1}
1	0 to 1/2 V_{CC1}

ANALOG GROUND (A.G) AND DIGITAL GROUND (D.G), PINS 1 AND 8

These are terminals for ground.
The analog circuitry and digital circuitry have seperate ground terminals, respectively.

POWER SUPPLIES (V_{CC2} AND V_{CC1}), PINS 15 AND 16

When the device operates within a voltage range of 3.5V to 6.0V, the power source is connected to V_{CC1} which is shorted to V_{CC2}.
When the device operates within a voltage range of 8V to 18V in case of DIP Packages and 8V to 13.2V in case of Flat Package, the power source is connected to V_{CC2}.
In this high voltage operation mode, the V_{CC1} pin is used as an output pin which supplies +5V stabilized voltage and 10mA load current and the supplied voltage is regurated in the internal voltage regurator.
V_{CC1} is used as the reference voltage of A/D conversion regardless any two types voltage.

ANALOG CIRCUIT CHARACTERISTICS FOR DIP PACKAGE

(V_{CC1} = V_{CC2} = 3.5V to 6.0V, T_A = 30°C to +85°C)

Parameter		Symbol	Condition	Value			Unit
				Min.	Typ.	Max.	
Resolution			–	–	–	8	Bit
Linearity Error			V_{CC1} = 5V	–	–	±0.5	LSB
Differential Linearity Error				–	–	±0.9	LSB
Zero Transition Voltage	Contracted Range	V_{ZC}	V_{CC1} = 5V, T_A = 25°C	0	6	16	mV
	Standard Range	V_{ZS}		7	17	27	mV
	Expanded Range	V_{ZE}		22	62	102	mV
Full Scale Transition Voltage	Contracted range	V_{FC}		600	625	650	mV
	Standard Range	V_{FS}		2.475	2.500	2.525	V
	Expanded Range	V_{FE}		9.600	10.000	10.400	V
Comparator Input Current		I_{IC}	V_{CC1} = 5V	-250	-100	–	nA
Divider Input Resistance for Expanded Range		R_{INE}	–	5	10	15	kΩ
Regulator	Output Voltage	V_{OR}	8V ≤ V_{CC2} ≤ 18V	4.5	5.0	5.5	V
	Line Regulation			–	4.0	–	mV/V
	Load Regulation		V_{CC2} = 12V, 0mA ≥ I_{out} ≥ -10mA	–	0.5	–	mV/mA
	Output Voltage Temperature		V_{CC2} = 12V	–	50	–	ppm/°C
Conversion Cycle Time		t_{CYC}	f_{CLK} = 100kHz	–	–	100	μs/ch

A minus sign (–) prefixed to a current value indicates that the current flows from the IC to the external circuit.

ANALOG CIRCUIT CHARACTERISTICS FOR CERAMIC DIP PACKAGE

(V_{CC1} = V_{CC2} = 3.5V to 6.0V, T_A = 30°C to +85°C)

Parameter		Symbol	Condition	Value			Unit
				Min.	Typ.	Max.	
Resolution			–	–	–	8	Bit
Linearity Error			V_{CC1} = 5V	–	–	±0.4	LSB
Differential Linearity Error				–	–	±0.8	LSB
Zero Transition Voltage	Contracted Range	V_{ZC}	V_{CC1} = 5V, T_A = 25°C	0	6	16	mV
	Standard Range	V_{ZS}		7	17	27	mV
	Expanded Range	V_{ZE}		22	62	102	mV
Full Scale Transition Voltage	Contracted range	V_{FC}		610	625	640	mV
	Standard Range	V_{FS}		2.480	2.500	2.520	V
	Expanded Range	V_{FE}		9.760	10.000	10.240	V
Comparator Input Current		I_{IC}	V_{CC1} = 5V	-250	-100	–	nA
Divider Input Resistance for Expanded Range		R_{INE}	–	5	10	15	kΩ
Regulator	Output Voltage	V_{OR}	8V ≤ V_{CC2} ≤ 18V	4.5	5.0	5.5	V
	Line Regulation			–	4.0	–	mV/V
	Load Regulation		V_{CC2} = 12V, 0mA ≥ I_{out} ≥ -10mA	–	0.5	–	mV/mA
	Output Voltage Temperature		V_{CC2} = 12V	–	50	–	ppm/°C
Conversion Cycle Time		t_{CYC}	f_{CLK} = 100kHz	–	–	100	μs/ch

A minus sign (–) prefixed to a current value indicates that the current flows from the IC to the external circuit.

ANALOG CIRCUIT CHARACTERISTICS FOR PLASTIC FLAT PACKAGE

(V_{CC1} = V_{CC2} = 3.5V to 6.0V, T_A = 30°C to +85°C)

Parameter		Symbol	Condition	Value			Unit
				Min.	Typ.	Max.	
Resolution			–	–	–	8	Bit
Linearity Error			V_{CC1} = 5V	–	–	±0.5	LSB
Differential Linearity Error				–	–	±0.9	LSB
Zero Transition Voltage	Contracted Range	V_{ZC}	V_{CC1} = 5V, T_A = 25°C	0	6	16	mV
	Standard Range	V_{ZS}		7	17	27	mV
	Expanded Range	V_{ZE}		22	62	102	mV
Full Scale Transition Voltage	Contracted range	V_{FC}		600	625	650	mV
	Standard Range	V_{FS}		2.475	2.500	2.525	V
	Expanded Range	V_{FE}		9.600	10.000	10.400	V
Comparator Input Current		I_{IC}	V_{CC1} = 5V	-250	-100	–	nA
Divider Input Resistance for Expanded Range		R_{INE}	–	5	10	15	kΩ
Regulator	Output Voltage	V_{OR}	8V ≤ V_{CC2} ≤ 13.2V	4.5	5.0	5.5	V
	Line Regulation			–	4.0	–	mV/V
	Load Regulation		V_{CC2} = 12V, 0mA ≥ I_{out} ≥ -2mA	–	0.5	–	mV/mA
	Output Voltage Temperature		V_{CC2} = 12V	–	50	–	ppm/°C
Conversion Cycle Time		t_{CYC}	f_{CLK} = 100kHz	–	–	100	μs/ch

A minus sign (–) prefixed to a current value indicates that the current flows from the IC to the external circuit.

DIGITAL CIRCUIT DC CHARACTERISTICS

(V_{CC1} = V_{CC2} = 3.5V to 6.0V, T_A = 30°C to +85°C)

Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Input Clamp Voltage	V_{IC}	V_{CC1} = 3.5V, I_{IL} = −18mA	—	—	−1.5	V
High Level Input Current	I_{OH}	V_{CC1} = 3.5V, V_{IH} = 2.0V, V_{IL} = 0.8V, V_{OH} = 20V	—	—	100	μA
Low Level Output Voltage	V_{OL1}	V_{CC1} = 3.5V, V_{IH} = 2.0V, V_{IL} = 0.8V, I_{OL} = 4mA	—	—	0.4	V
	V_{OL2}	V_{CC1} = 3.5V, V_{IH} = 2.0V, V_{IL} = 0.8V, I_{OL} = 8mA	—	—	0.5	V
High Level Input Current	I_{IH1}	V_{CC1} = 6.0V, V_{IH} = 2.7V	—	—	20	μA
	I_{IH2}	V_{CC1} = 6.0V, V_{IH} = 20V	—	—	100	μA
Low Level Input Current	I_{IL}	V_{CC1} = 6.0V, V_{IL} = 0.4V	—	−50	−150	μA
Power Supply Current for V_{CC1}	I_{CC1}	V_{CC1} = 6.0V	—	15*	30	mA
Power Supply Current for V_{CC2}	I_{CC2}	V_{CC1} = Open, V_{CC2} = 20V for DIP Package V_{CC2} = 13.2V for FLAT Package	—	15	25	mA

***Note:** This typical value is measured at V_{CC1} = 5.0V and T_A = 25°C.
A minus sign (−) prefixed to a current value indicates that the current flows from the IC to the external circuit.
The values are measured at V_{CC1} = V_{CC2} except the I_{CC2} parameter of .

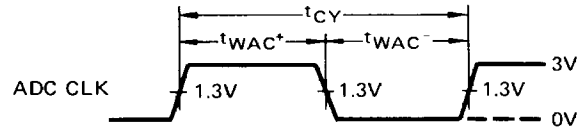
DIGITAL CIRCUIT AC CHARACTERISTICS

(V_{CC1} = V_{CC2} = 3.5V to 6.0V, T_A = 30°C to +85°C)

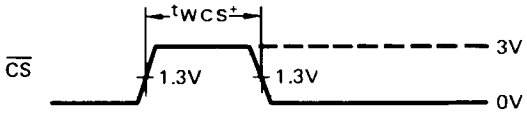
Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
ADC CLK Cycle Time	t_{CY}	10	—	—	μs
ADC CLK H Level Pulse Width	t_{WAC+}	2.5	—	—	μs
ADC CLK L Level Pusle Width	t_{WAC-}	2.5	—	—	μs
$\overline{CS}$ H Level Pulse Width	t_{WCS+}	1.5	—	—	μs
$\overline{CS}$ Set-up Time	t_{SCS}	1	—	—	μs
$\overline{CS}$ Hold Time	t_{HCS}	1	—	—	μs
Channel Set-up Time	t_{SCH}	0	—	—	μs
Channel Hold Time	t_{HCH}	1	—	—	μs
Propagation Delay Time	t_{PLH} t_{PHL}	—	800	2,000	ns

Fig. 2 – AC CHARACTERISTICS WAVEFORM

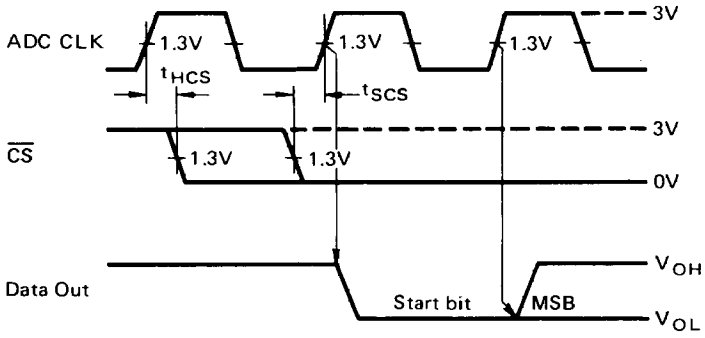
(1) ADC CLK



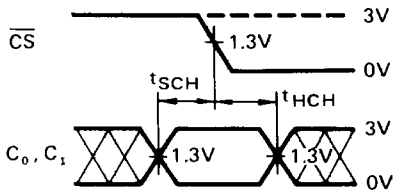
(2) $\overline{CS}$



(3) $\overline{CS}$ Set-up/Hold Time



(4) Channel Set-up/Hold Time



(5) Propagation Delay Time

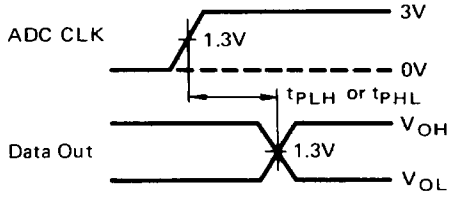
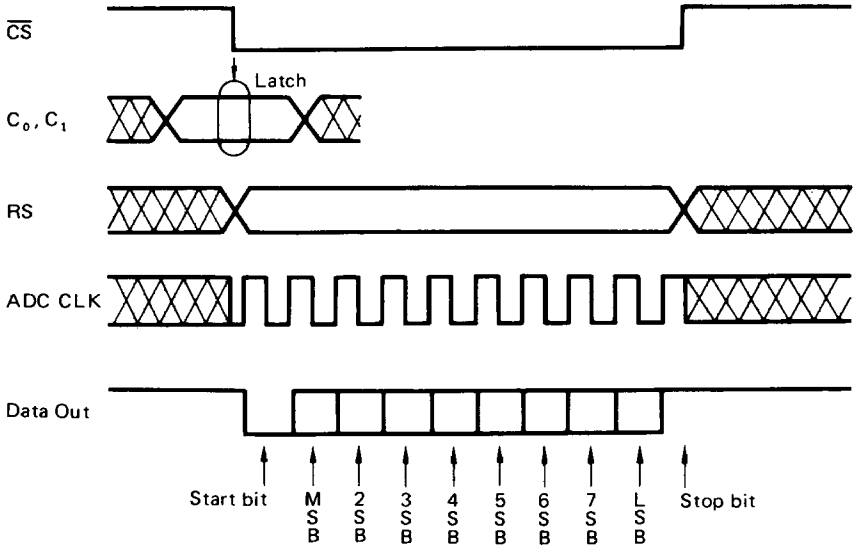
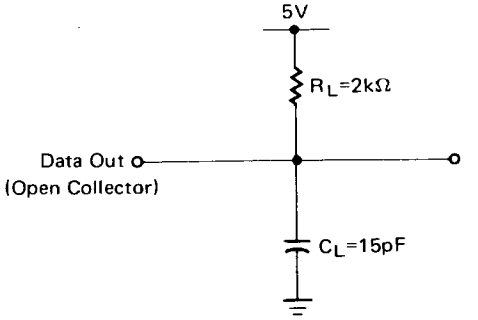


Fig. 3 – TIMING DIAGRAM



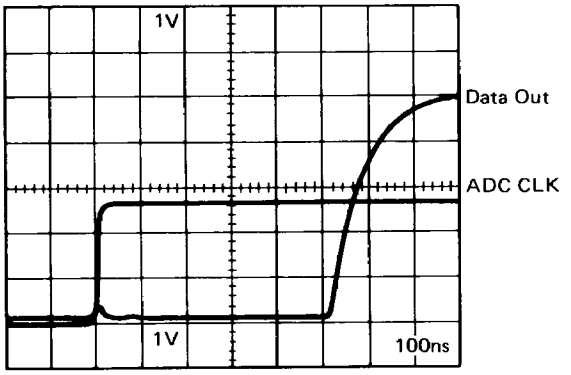
Note: RS should be held to one ranged "1" or "0" until data conversion is completed.

Fig. 4 – LOAD CONDITIONS

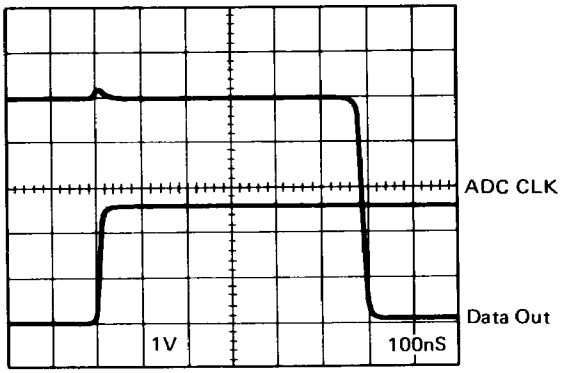


TYPICAL WAVEFORMS OF PROPAGATION DELAY

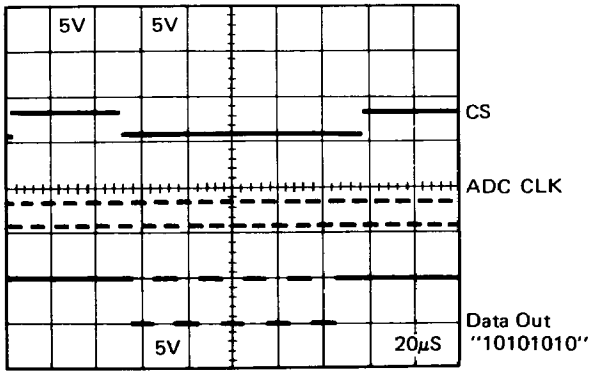
t_{PLH} (Data Out Transition from low-level to high-level)



t_{PHL} (Data Out Transition from high-level to low-level)

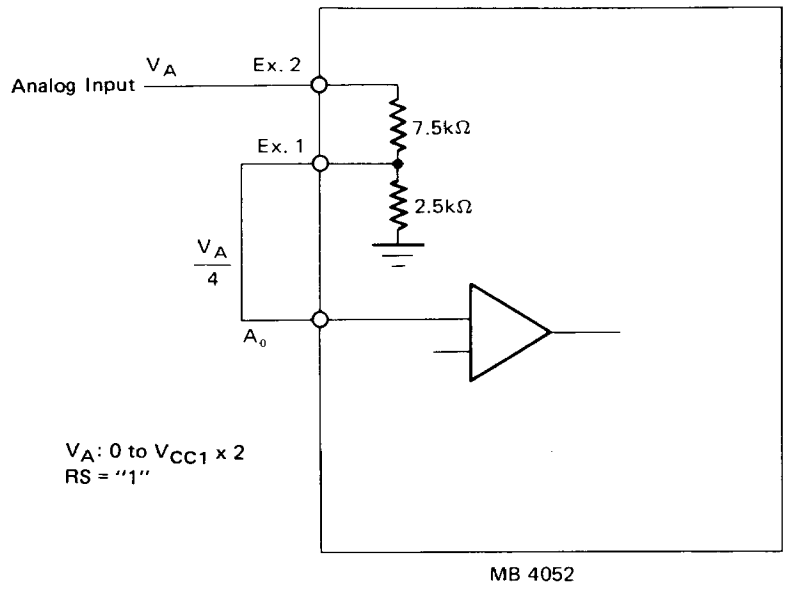


TYPICAL CONVERSION WAVEFORM



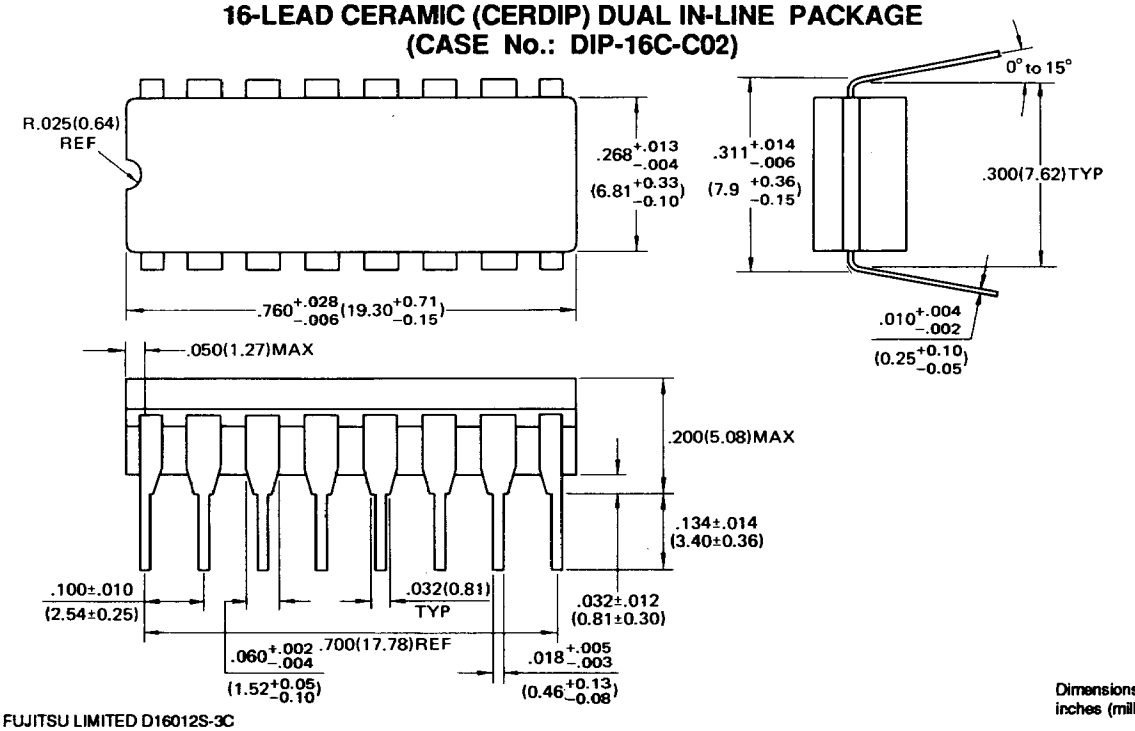
Condition
f_{CLK} = 100kHz
V_{CC1} = 5V
Standard Range
$V_{IA} \doteqdot$ 1663 mV

Fig. 5 – EXAMPLE OF EXPAND RANGE MODE CONNECTION



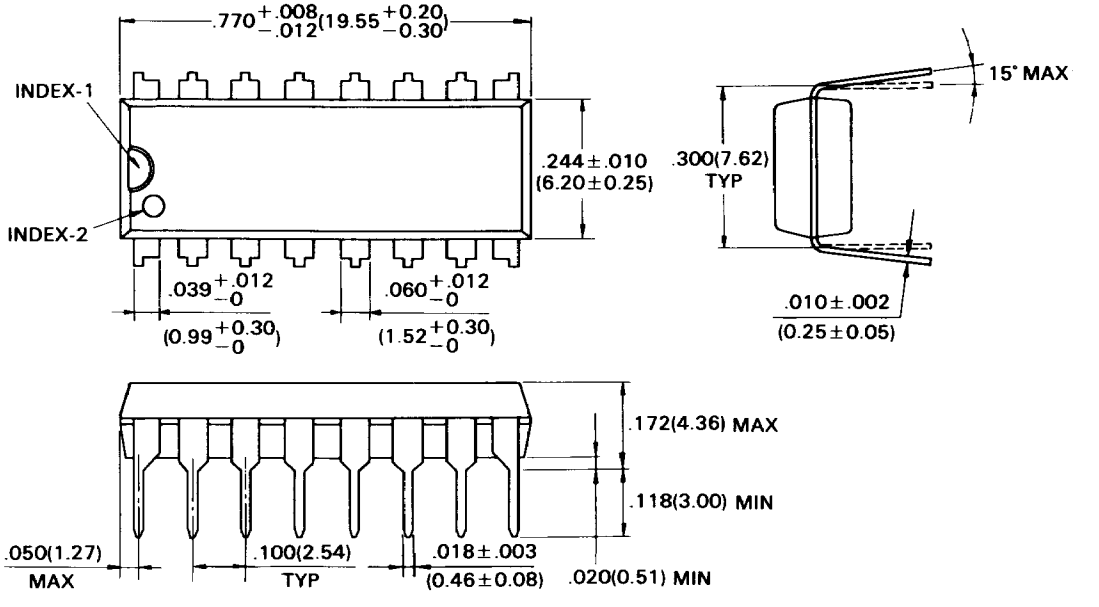
PACKAGE DIMENSIONS

16-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
(CASE No.: DIP-16C-C02)



Dimensions in inches (millimeters)

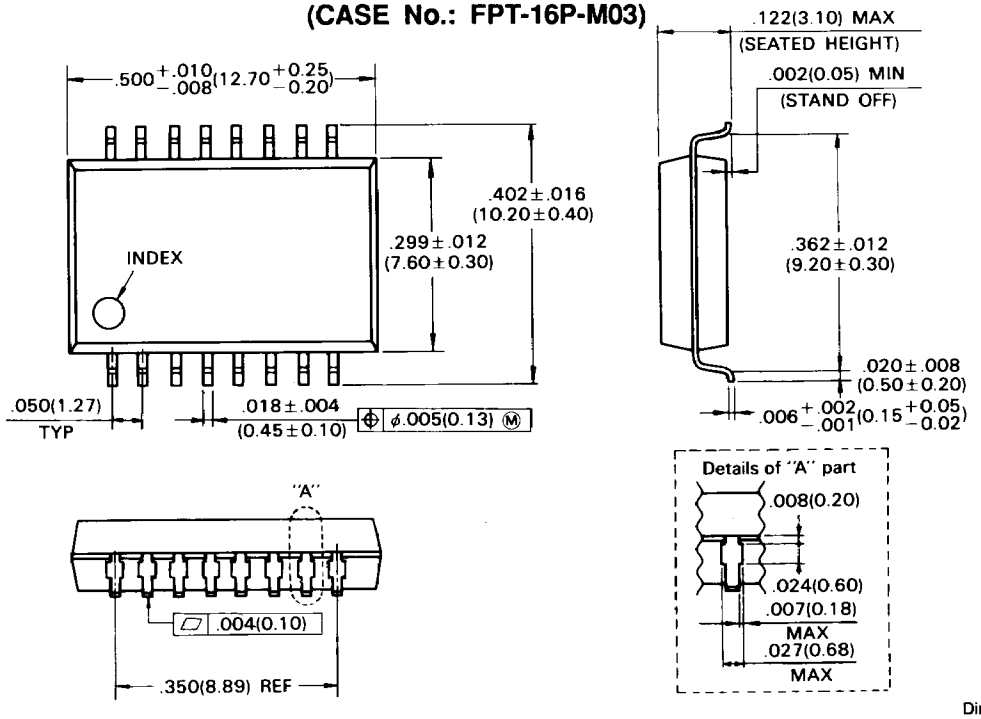
16-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-16P-M04)



Dimensions in inches (millimeters)

PACKAGE DIMENSIONS (Continued)

16-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-16P-M03)



Dimensions in inches (millimeters)

FUJITSU LIMITED

For further information please contact:

Japan
FUJITSU LIMITED
Integrated Circuits and Semiconductor Marketing
Furukawa Sogo Bldg., 6–1, Marunouchi 2–chome
Chiyoda–ku, Tokyo 100, Japan
Tel: (03) 216–3211
Telex: 781–2224361
FAX: (03) 216–9771

North and South America
FUJITSU MICROELECTRONICS, INC.
Integrated Circuits Division
3545 North First Street
San Jose, CA 95134–1804 USA
Tel: 408–922–9000
Telex: 910–338–0190
FAX: 408–432–9044

Europe
FUJITSU MIKROELEKTRONIK GmbH
Arabella Centre 9. OG
Lyoner Strasse 44–48
D–6000 Frankfurt 71
F.R. Germany
Tel: (069) 66320
Telex: 411963
FAX: (069) 6632122

Asia
FUJITSU MICROELECTRONICS ASIA PTE LIMITED
#06–04 to #06–07
Plaza By The Park
No. 51 Bras Basah Road
Singapore 0719
Tel: 336–1600
Telex: 55573
FAX: 336–1609

017373

Printed in Japan PV0077–902A5