

**SONY**

# CXP5014/CXP5016

## CMOS 4-bit 1 Chip Microcomputer

### Description

CXP5014/CXP5016 is a CMOS 4-bit microcomputer which consists of 4-bit CPU, ROM, RAM, I/O port, 8-bit timer, 8-bit timer/counter, 18-bit time base timer, 8-bit serial I/O, vector interruption, power on reset function, fluorescent display tube controller/driver, D/A conversion PWM output port. They are integrated into a single chip with the standby function, etc. which are to be operated at a low power consumption.

### Features

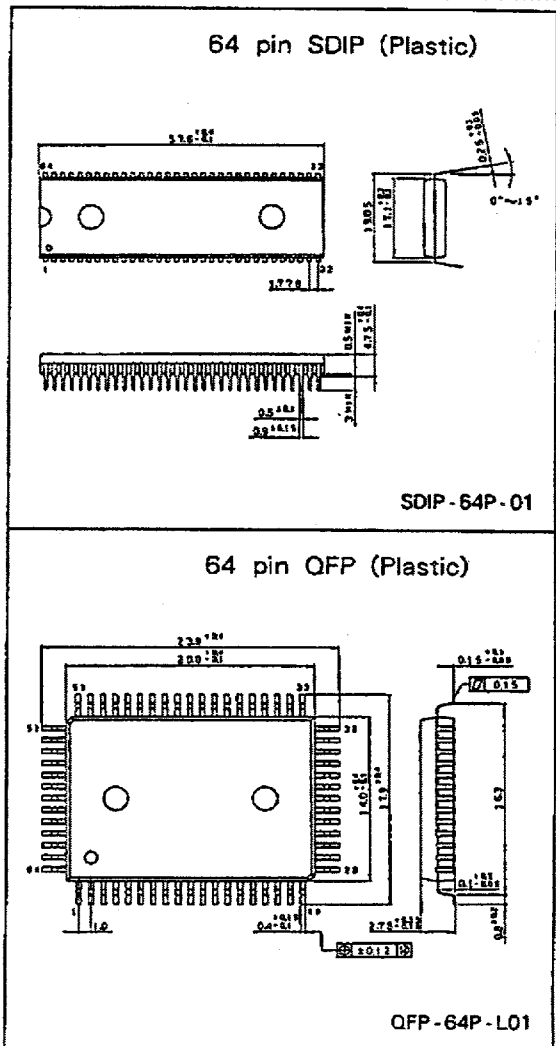
- Instruction cycle 3.8  $\mu$ s/4.19MHz  
1.9  $\mu$ s/4.19MHz  
(High speed version)
- ROM capacity 6,144  $\times$  8 bits (CXP5016)  
4,096  $\times$  8 bits (CXP5014)
- RAM capacity 288  $\times$  4 bits
- 32 general purpose I/O ports
- Fluorescent display tube controller/driver  
(Able to display maximum 144 segments)
  - 1 to 16 digits dynamic scan display
  - Page mode/variable mode
  - Dimmer function
  - High tension proof output (40V)
  - Selection possible for incorporating pull-down resistance (mask option)
- 14-bit PWM output for D/A conversion
- Remote control receiving circuit
- 2 external interruption input pins  
(Except for QFP)
- 8-bit/4-bit variable serial I/O
- 8-bit timer, 8-bit timer/event counter and 18-bit time base timer, independently controlled
- Arithmetic and logical operations possible between the entire RAM area, I/O area and the accumulator by means of memory mapped I/O
- Reference to the entire ROM area is possible with the table look-up instruction
- 2 kinds of power down modes of sleep and stop
- Power on reset circuit (mask option)
- Provided with 64 pin plastic SDIP/QFP
- Provided with 64 pin piggyback SDIP/QFP (CXP5010)

### Structure

Silicon gate CMOS IC

### Package Outline

Unit : mm

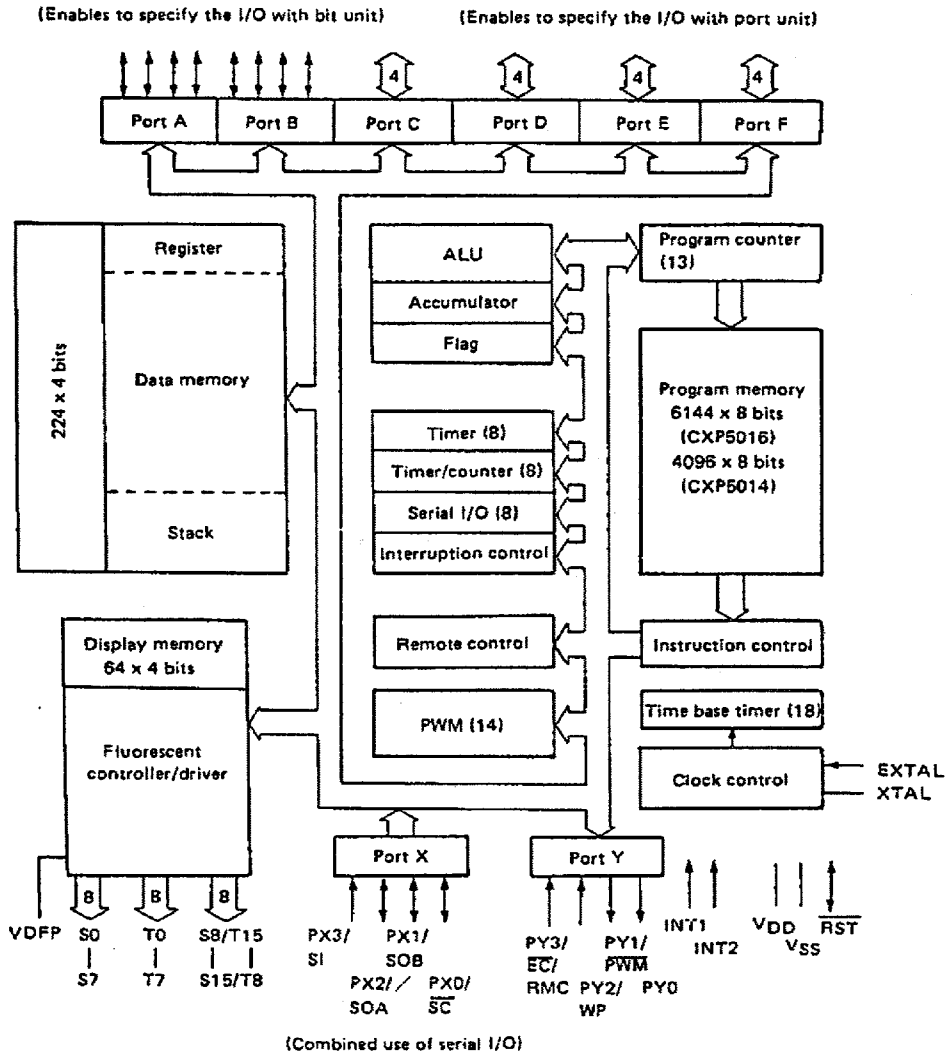


SONY reserves the right to change products and specifications without notice.  
This information does not convey any license under patent rights of SONY corporation or others.

60179A - ST

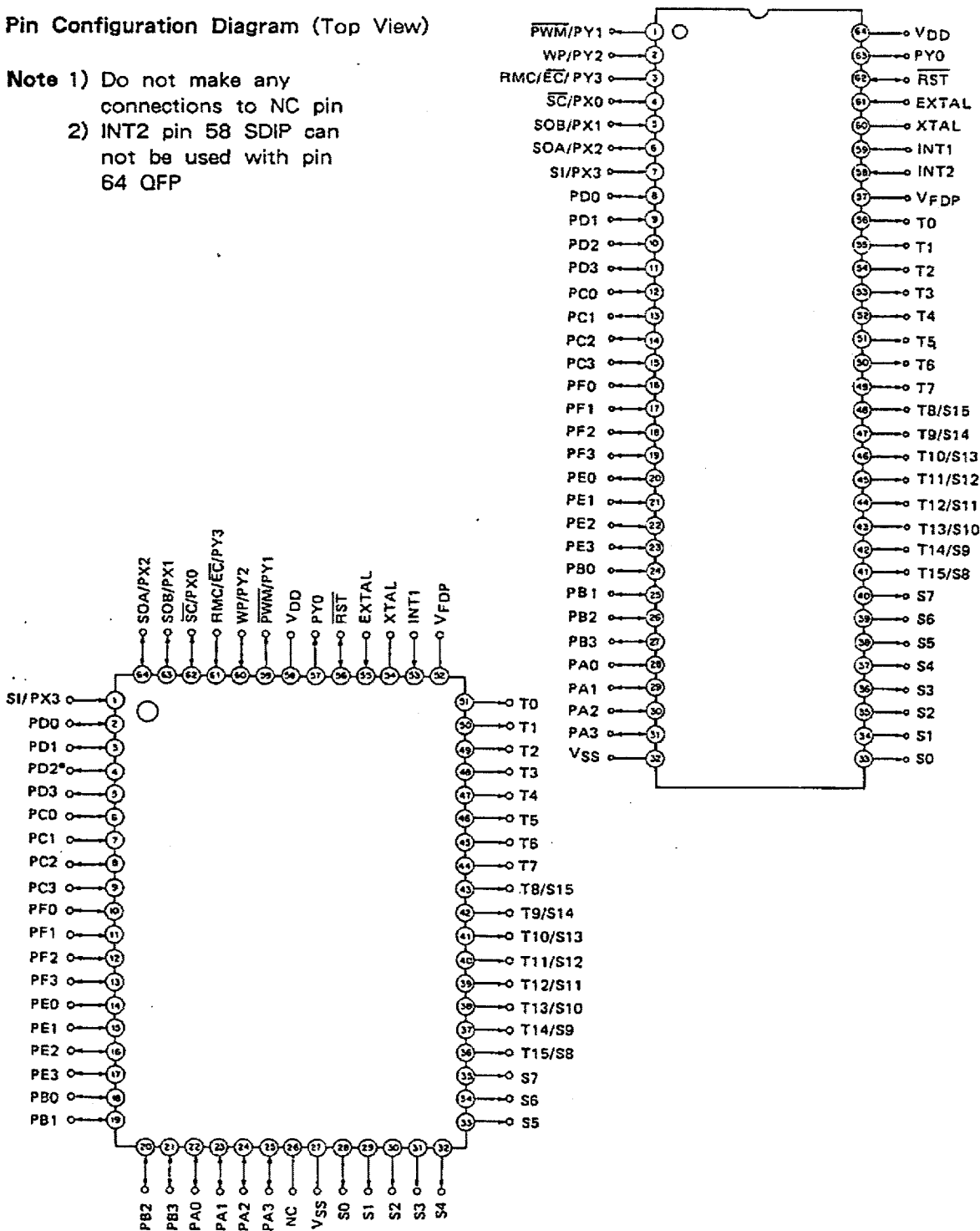
8382383 0017212 733

Block Diagram



Pin Configuration Diagram (Top View)

- Note** 1) Do not make any connections to NC pin  
 2) INT2 pin 58 SDIP can not be used with pin 64 QFP



## Absolute Maximum Ratings

Ta = -20°C to +75°C, Vss = 0V

Item	Symbol	Rating	Unit	Remarks
Power supply voltage	V <sub>DD</sub>	-0.3 to +7.0	V	
Input voltage	V <sub>IN</sub>	-0.3 to +7.0*1	V	
Output voltage	V <sub>OUT</sub>	-0.3 to +7.0*1	V	
Display output voltage	V <sub>OD</sub>	V <sub>DD</sub> - 40 to V <sub>DD</sub> + 0.3	V	As P channel transistor is open drain, V <sub>DD</sub> voltage is determined as standard.
High level output current	I <sub>OH</sub>	-10	mA	Other than display output pins*2: per pin
	I <sub>ODH1</sub>	-15	mA	Display output S0 to S7: per pin
	I <sub>ODH2</sub>	-30	mA	Display output T0 to T7, T8/S15 to T15/S8: per pin
High level total output current	Σ I <sub>OH</sub>	-40	mA	Total of other than display output pins
	Σ I <sub>ODH</sub>	-60	mA	Total of display output pins
Low level output current	I <sub>OL</sub>	17	mA	Port 1 pin
Low level total output current	Σ I <sub>OL</sub>	50	mA	Entire pin total
Operating temperature	T <sub>opr</sub>	-20 to +75	°C	
Storage temperature	T <sub>stg</sub>	-55 to +150	°C	
Allowable power dissipation	P <sub>D</sub>	1000	mW	SDIP
		600	mW	QFP

Note) Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should better take place under the recommended operation conditions. Exceeding those conditions may adversely affect the reliability of the LSI.

\*1) V<sub>IN</sub> and V<sub>OUT</sub> should not exceed V<sub>DD</sub> + 0.3V.

\*2) Specifies the output current of the general purpose I/O port PA to PF, PX0 to PX2, PY0 and PY1.

## Recommended Operating Condition

Vss = 0V

Item	Symbol	Min.	Max.	Unit	Remarks
Power supply voltage	V <sub>DD</sub>	4.5	5.5	V	Guaranteed range during operation
		3.5	5.5	V	Guaranteed data hold operation range during STOP
High level input voltage	V <sub>IH</sub>	0.7V <sub>DD</sub>	V <sub>DD</sub>	V	
	V <sub>IHS</sub>	0.8V <sub>DD</sub>	V <sub>DD</sub>	V	Hysteresis input*1
	V <sub>IHEX</sub>	V <sub>DD</sub> - 0.4	V <sub>DD</sub> + 0.3	V	EXTAL pin*2
Low level input voltage	V <sub>IL</sub>	0	0.3V <sub>DD</sub>	V	
	V <sub>ILS</sub>	0	0.2V <sub>DD</sub>	V	Hysteresis input*1
	V <sub>ILEX</sub>	-0.3	0.4	V	EXTAL pin*2
Operating temperature	T <sub>opr</sub>	-20	+75	°C	

\*1) They are the respective pins of INT1, INT2, PX0, PX3, PY2, PY3 and RST.

\*2) Specified only during external clock input.

## Electrical Characteristics

## DC characteristics

Ta = -20°C to +75°C, Vss = 0V

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
High level output voltage	V <sub>OH</sub>	PA to PF PX0 to PX2	V <sub>DD</sub> = 4.5V, I <sub>OH</sub> = -0.5mA	4.0			V
			V <sub>DD</sub> = 4.5V, I <sub>OH</sub> = -1.2mA	3.5			V
Low level output voltage	V <sub>OL</sub>	PY0, PY1 $\overline{\text{RST}}$ (V <sub>OL</sub> only)	V <sub>DD</sub> = 4.5V, I <sub>OL</sub> = 1.8mA			0.4	V
			V <sub>DD</sub> = 4.5V, I <sub>OL</sub> = 3.6mA			0.6	V
Input current	I <sub>IH</sub>	EXTAL	V <sub>DD</sub> = 5.5V, V <sub>IH</sub> = 5.5V	0.5		40	μA
	I <sub>IIE</sub>		V <sub>DD</sub> = 5.5V	-0.5		-40	μA
	I <sub>ILR</sub>		$\overline{\text{RST}}$ *2	V <sub>I</sub> = 0.4V	-1.5		-400
High impedance I/O leakage current	I <sub>Iz</sub>	PA to PF, PX0 to PX3, PY2, PY3, INT1, INT2, $\overline{\text{RST}}$ *2	V <sub>DD</sub> = 5.5V V <sub>I</sub> = 0, 5.5V			±10	μA
Display output current	I <sub>OH</sub>	S0 to S7	V <sub>DD</sub> = 4.5V V <sub>OH</sub> = V <sub>DD</sub> - 2.5V	-7			mA
		S8/T15 to S15/ T8, T0 to T7		-15			mA
Open drain output leakage current (P-CH Tr OFF in state)	I <sub>IOL</sub>	S0 to S7, S8/T15 to S15/T8, T0 to T7	V <sub>DD</sub> = 5.5V V <sub>OL</sub> = V <sub>DD</sub> - 35V			-20	μA
Pull-down resistance*1	R <sub>L</sub>	S0 to S7, S8/T15 to S15/T8, T0 to T7	V <sub>DD</sub> = 5V V <sub>FDP</sub> = V <sub>DD</sub> - 35V	60		270	kΩ
Supply current	I <sub>DD</sub>	V <sub>DD</sub>	Crystal oscillation (C1 = C2 = 22pF) of V <sub>DD</sub> = 5.5V, 4.19MHz entire output pins open		5 (7)*3	15 (20)*3	mA
	I <sub>DDSP</sub>				3 (5)*3	9 (12)*3	mA
	I <sub>DDs</sub>					10	μA
Input capacity	C <sub>IN</sub>	Other than S0 to S7, S8/T15 to S15/T8, T0 to T7, Vss, V <sub>DD</sub> pins	Clock 1MHz 0V other than the measured pins		10	20	pF

\*1) In case the incorporated pull-down resistance has been selected with mask option.

\*2)  $\overline{\text{RST}}$  pin specifies the input current when the pull-up resistance is selected, and specifies leakage current when nonresistance is selected.

\*3) Specifies the power supply current of the high speed version.

AC Characteristics

(1) Clock timing

Ta = -20°C to +75°C, VDD = 4.5V to 5.5V, VSS = 0V

Item	Symbol	Pin	Condition	Min.	Max.	Unit
System clock frequency	fc	XTAL EXTAL	Fig. 1, Fig. 2	1	5	MHz
System clock input pulse width	txL	EXTAL	Fig. 1, Fig. 2 (External clock drive)	90		ns
	txH					
System clock input rising and falling times	tCR				200	ns
	tCF					
Event count clock input pulse width	tEL tEH	EC	Fig. 3	tsys*1 + 0.05		μs
Event count clock input rising and falling times	tER tEF	EC	Fig. 3		20	ms

\*1) tsys in the standard version is  $t_{sys} = 16/f_c$   
 tsys in the high speed version is  $t_{sys} = 8/f_c$

Note) When adjusting the frequency accurately, there may be cases in which they may differ from Fig. 2.

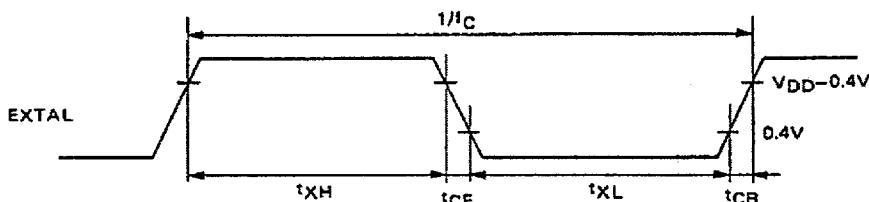


Fig. 1 Clock timing

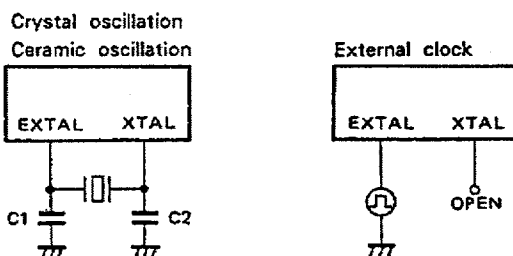


Fig. 2 Clock applying condition

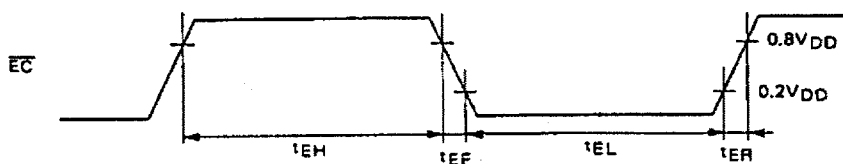


Fig. 3 Event count clock timing

(2) Serial transfer

Ta = -20°C to +75°C, VDD = 4.5V to 5.5V, VSS = 0V

Item	Symbol	Pin	Condition	Min.	Max.	Unit
Serial transfer clock ( $\overline{SC}$ ) cycle time	tkcy	$\overline{SC}$	Input mode	$t_{sys}/4 + 1.42$		$\mu s$
			Output mode	$t_{sys}$		$\mu s$
Serial transfer clock ( $\overline{SC}$ ) high and low level widths	tkh tkl	$\overline{SC}$	Input mode	$t_{sys}/8 + 0.7$		$\mu s$
			Output mode	$t_{sys}/2 - 0.1$		$\mu s$
Serial data input setup time (against $\overline{SC}$ $\uparrow$ )	tsik	SI	$\overline{SC}$ input mode	0.1		$\mu s$
			$\overline{SC}$ output mode	0.2		$\mu s$
Serial data input hold time (against $\overline{SC}$ $\uparrow$ )	tksi	SI	$\overline{SC}$ input mode	$t_{sys}/8 + 0.5$		$\mu s$
			$\overline{SC}$ output mode	0.1		$\mu s$
Data delay time from $\overline{SC}$ falling	tksoa	SOA			$t_{sys}/8 + 0.5$	$\mu s$
	tksoB	SOB			$t_{sys}/8 + 0.5$	$\mu s$

- Note 1)  $t_{sys}$  in the standard version is  $t_{sys} = 16/f_c$   
 $t_{sys}$  in the high speed version is  $t_{sys} = 8/f_c$   
 2) The Load of data output delay is  $50pF + 1TTL$

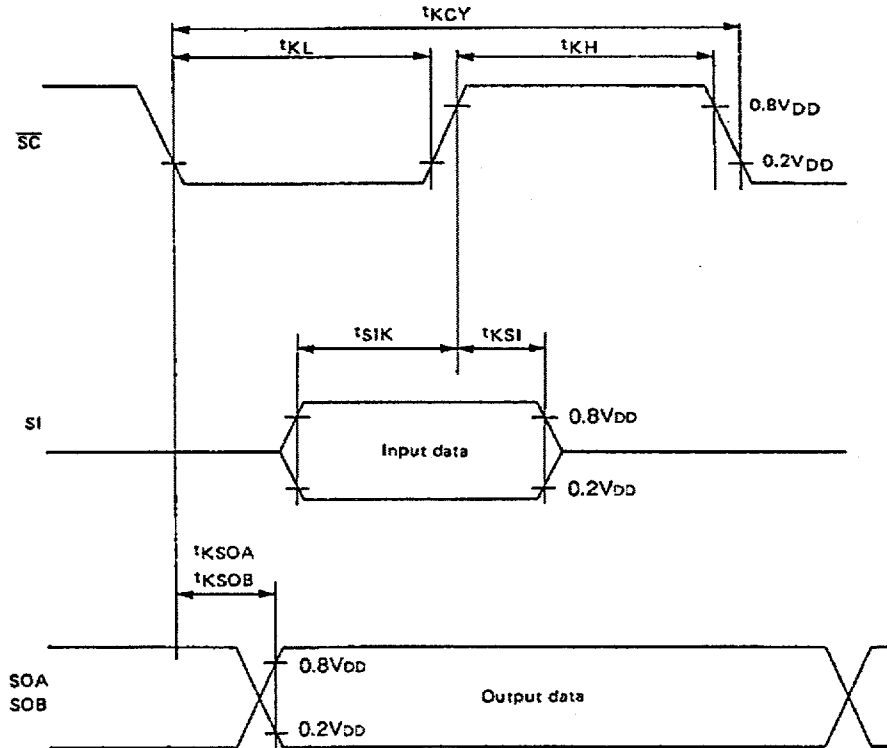


Fig. 4 Serial transfer timing

(3) Others

Ta = -20°C to +75°C, VDD = 4.5V to 5.5V, VSS = 0V

Item	Symbol	Pin	Condition	Min.	Max.	Unit
External interruption high and low level widths	t11H, t11L	INT1	During edge detection mode	tsys + 0.05		μs
	t12H, t12L	INT2*1		tsys + 0.05		μs
Reset input low level width	trSL	RST		2tsys		μs
Wake-up input high level width	twPH	WP	STOP mode	500		ns
			SLEEP mode	tsys + 0.05		μs

Note) tsys in the standard version is tsys = 16/fc  
 tsys in the high speed version is tsys = 8/fc

\*1) Specified only SDIP type.

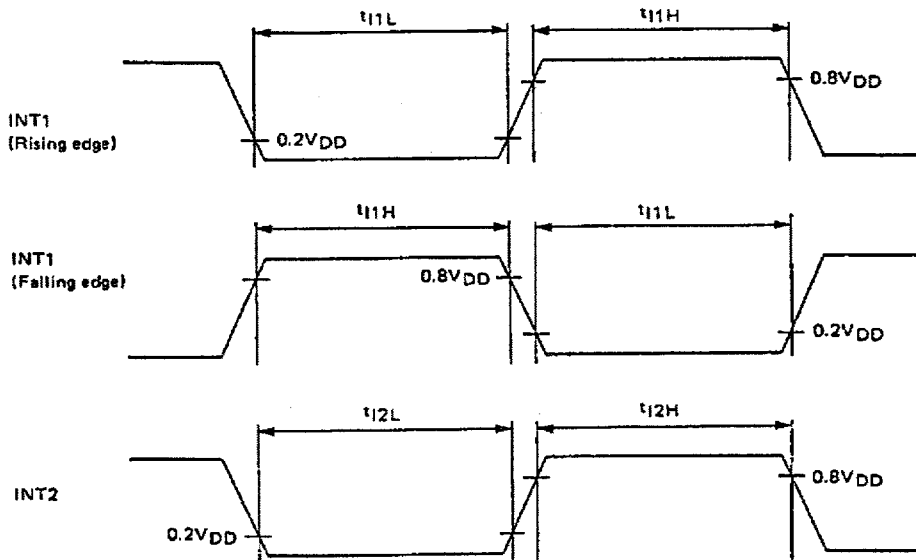


Fig. 5 Interruption input timing

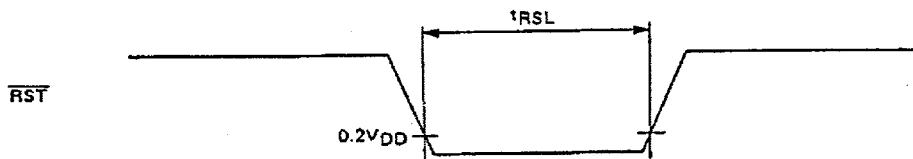


Fig. 6 Reset input timing

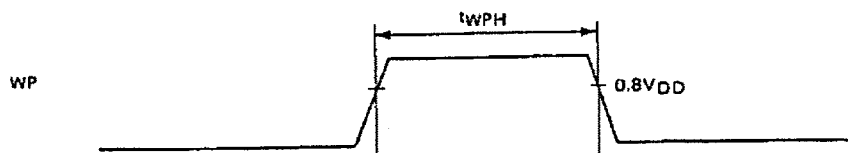


Fig. 7 Wake-up input timing



Power on reset \*

Ta = -20°C to +75°C, Vss = 0V

Item	Symbol	Pin	Condition	Min.	Max.	Unit
Power supply rising time	t <sub>R</sub>	V <sub>DD</sub>	Power on reset	0.05	50	ms
Power supply cut-off time	t <sub>OFF</sub>		Repetitive power on reset	1		ms

\* Specifies only when power on reset function is selected.



Raise the power supply smoothly.

Fig. 8 Power on reset

Notes on Application

See Fig. 9, Additive capacity calculation chart, when using the crystal oscillator and select the appropriate capacity.

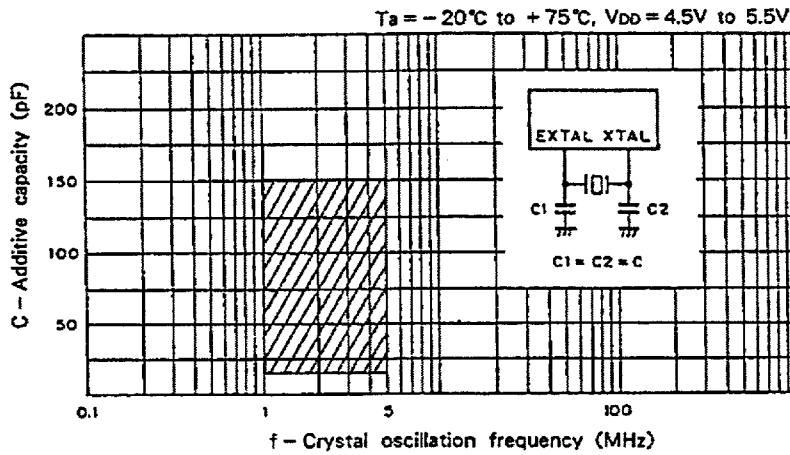


Fig. 9 Crystal oscillation circuit additive capacity calculation chart

**Note)** The above chart shows a range in which the average quartz resonator has a relatively fast oscillation rising edge and stable characteristics. The capacity should be selected to correspond to the appropriate constant for each quartz resonator, should the frequency of the quartz resonator be constant.

