Monolithic Digital AM/FM Receiver Radio-on-a-Chip™

KT0923

Features

Worldwide full band FM/AM support
- FM: 32MHz-110MHz
- MW: 500KHz-1710KHz

Fully integrated frequency synthesizer with no external components

High Sensitivity
- 1.6uVEMF for FM
- 16uVEMF for AM

High Fidelity
- SNR (FM/AM): 60dB/55dB
- THD: 0.3%

Low Supply Current
- 25mA (operating)
- <15uA (standby)

Advanced features
- Automatic antenna tuning
- Adjustable AM channel filters (1/2/3/4/5KHz)
- Enhanced Automatic Frequency Control (AFC) Capability (up to 200kHz)
- Flexible AM Automatic Gain Control (AGC)
- Embedded AM/FM SNR meter
- Embedded ST indicator
- Embedded line-in driver and TPDT switch.
- Fast seek/Tune
- Integrated stereo headphone driver
- I2C control interface for MCU
- Channel and volume info stored and recovered

Low supply voltage
- 2.1V to 3.6V, can be supplied by 2 AAA batteries

Support both 32.768KHz and 38KHz crystal

True Continuous Reference Clock supported
- From 30KHz to 40MHz with 3V voltage tolerance

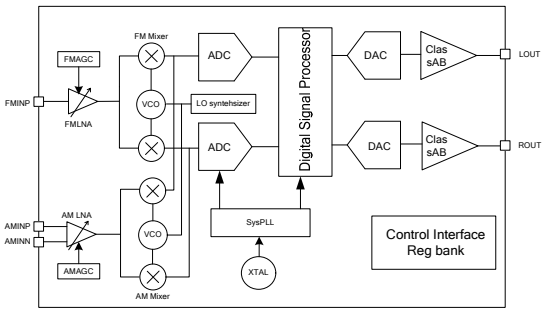
Compatible with EN55020

Small form factor SSOP20L package

RoHS Compliant

Applications

Desktop and portable radio, mini/portable audio systems, clock radio, campus radio, PMP docking station, car audio system, toy and gift.



KT0923 System Diagram

Description

The KT0923 is KT Micro's 2nd generation of proprietary fully integrated AM/FM receiver chip that upgrades the performance, improve the user experience and ease integration and manufacturing efforts. The new features includes the additional audio input, independent status indicator, improved EMI/EMC and higher FM stereo separation.

Thanks to the patented tuning technology, the receiver maintains good signal reception even with short antennas. The chip consumes merely 25mA current and can be powered by 2 AAA batteries. Another useful feature is that the volume and channel information can be preserved in standby mode without external memories. KT0923 supports a wide range of reference clocks from 32.768KHz to 26MHz, hence can share system clocks with a varieties of MCUs further reducing the system BOM cost. The KT0923 have different user interface schemes like other parts in the KT092x family,

With high audio performance, fully integrated features and low BOM cost, KT0923 is ideal for various applications and products that requires flexible programbility for rich features.

Rev. 1.0

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1. Electrical Specification

Table 1: Operation Condition

Parameter	Symbol	Operating Condition	Min	Typ	Max	Units
Power Supply	AVDD	Relative to AVSS	2.1	3.3	3.6	V
Ambient Temperature	Ta		-30	25	70	℃

Table 2: DC Characteristics

Parameter		Symbol	Test/Operating Condition	Min	Typ	Max	Units
Current Consumption	FM Mode	I_{FM}		-	24	-	mA
	AM Mode	I_{AM}			26		mA
Standby Current		I_{APD}			15		μA

Table 3: FM Receiver Characteristics

(Unless otherwise noted Ta = -30~70℃, VDD= 2.1V to 3.6V)

Parameter	Symbol	Test/Operating Condition	Min	Typ	Max	Units
FM Frequency Range	F_{rx}		32		110	MHz
Sensitivity[1,2,3]	Sen	(S+N)/N=26dB		1.6	2	uVemf
Input referred 3rd Order Intermodulation Production[4,5]	IIP3			85		dBuVEMF
Adjacent Channel Selectivity		±200KHz	35		51	dB
Alternate Channel Selectivity		±400KHz	50		70	dB
Image Rejection Radio				35		dB
AM suppression				50		dB
RCLK frequency			30	32.768	40,000	KHz
RCLK frequency Range[8]			-100		100	ppm
Audio Output Voltage[1,2,3,4]		32ohm load	-	96	-	mV_{RMS}
Audio Band Limits[1,2,4]		±3dB	30		15k	Hz
Audio Stereo Separation [1,4,6]			40			dB
Audio Mono S/N[1,2,3,4]			55	60		dB
Audio Stereo S/N[1,4,6,7]		DBLND=1		64		dB
Audio THD[1,2,4,6]				0.3		%
De-emphasis Time Constant		DE=0		75		μs
		DE=1		50		μs
Audio Common Mode Voltage				0.85		V
Audio Output Load Resistance	R_L	Single-ended		32		Ω
Seek/Tune Time					50	ms
Power-up Time					600	ms

Notes:
1. FMOD=1KHz, 75us de-emphasis
2. MONO=1
3. △F=22.5KHz
4. V_{EMF}=1mV, Frx=32MHz~110MHz
5. AGCD=1
6. △F=75KHz
7. VOLUME<4:0>=11111
8. The supported RCLK frequency is not continuous. Please refer to application notes.

Table 4: AM Receiver Characteristics

(Unless otherwise noted Ta = -30~70℃, VDD= 2.1V to 3.6V)

Parameter	Symbol	Test/Operating Condition	Min	Typ	Max	Units
AM Frequency Range	F_{rx}		500		1710	KHz
Sensitivity[1,2]	Sen	(S+N)/N=26dB		15		uVemf
Audio Output Voltage[1,2,3,4]		32ohm load		96		mV_{RMS}
Audio Mono S/N[1,2,3,4]				55		dB
Audio THD[1,2,4,6]				0.3	0.6	%
Antenna inductance	L		250	300	350	uH

Notes:
1. FMOD=1KHz
2. Modulation index is 30%
3. V_{EMF}=1mV, Frx=500KHz~1710KHz
4. VOLUME<4:0>=11111

2. Pin List

Table 5. Pin list

Pin Num	Pin Name	Description
1	LINE_CL	Left channel input of line in C.
2	LINE_BR	Right channel input of line in B.
3	LINE_BL	Left channel input of line in B.
4	LINE_AR	Right channel input of line in A.
5	LINE_AL	Left channel input of line in A.
6	ROUT	Right channel audio output.
7	LOUT	Left channel audio output.
8	AVSS	Analog ground.
9	AVDD	Power supply.
10	XI/RCLK	Crystal input/Reference clock input.
11	XO	Crystal output.
12	AMINP	AM RF positive input.
13	AMINN	AM RF negative input.
14	RFINP	FM RF input.
15	RFGND	RF ground.
16	DVSS	Digital ground.
17	ST	ST indicator.
18	SCL	SCL of I2C interface. Tied to an internal 47kohm pull-up resistor.
19	SDA	SDA of I2C interface. Tied to an internal 47kohm pull-up resistor.
20	LINE_CR	Right channel input of line in C.

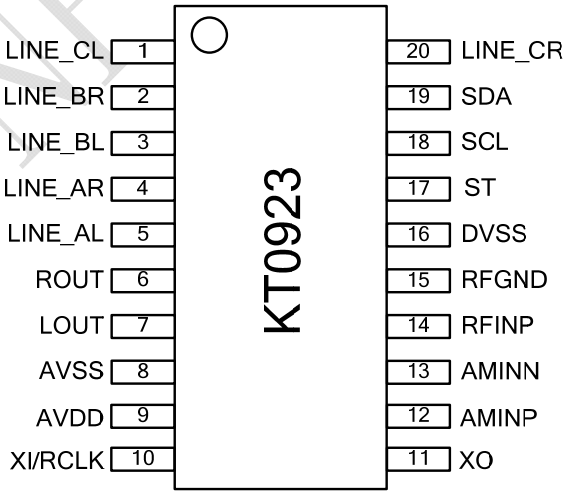


Figure 1. KT0923 Pin assignment (Top view)

3. Function Description

3.1. Overview

KT0923 offers a true single-chip, full-band FM/AM and versatile radio solution by minimizing the external components and offering a variety of configurations.

3.2. FM Receiver

KT0923 enters FM mode by setting register AM_FM to 0. The FM receiver is based on the architecture of KT Micro's latest generation FM receiver chips in mass production. There are no external filters or frequency-tuning devices thanks to a proprietary digital low-IF architecture consisting of a fully-integrated LNA, an automatic gain control (AGC), a set of high-performance ADCs, high-quality analog and digital filters, and an on-chip low-noise self-tuning VCO. The on-chip high-fidelity Class-AB driver further eliminates the need for external audio amplifiers and can drive stereo headphones directly.

3.3. AM Receiver

KT0923 enters AM mode by setting register AM_FM to 1. The AM Receiver employs a similar digital low IF architecture and share many circuits with the FM receiver. The AM receiver supports a wide band from 500KHz to 1710KHz also known as the popular AM bands. The minimum AM channel spacing can be set to 1KHz. The bandwidth of the channel filter can be set to 1KHz to 5KHz to suit various requirements.

The AM receiver in KT0923 can provide accurate and automatic AM tuning without manual alignment. It supports 300uH ferrite loop antenna with +/- 25% tolerance.

3.4. Operation Bands

KT0923 supports wide FM band and AM bands. The FM receiver covers frequencies from 32MHz to 110MHz. The MW band is from 500KHz to 1710KHz.

3.5. Standby

To enter standby mode, the STDBY register shall be set to 1 through I2C interface. In standby mode, the channel, volume and band information will be preserved within the chip.

3.6. Crystal and reference clock

KT0923 integrates a low frequency crystal oscillator that supports 32.768KHz or 38KHz crystals. Alternatively a CMOS level external reference clock may be used by setting the RCLK_EN register to 1 and setting XTAL_FREQ<25:0> according to the frequency of

the reference clock. The XTAL_FREQ<25:0> is the frequency value in the unit of Hz. In order to illuminate the usage of these bits clearly some examples are given in Table 6.

Table 6. Examples using different crystal or reference clock

	RCLK_EN	XTAL_FREQ <25:16>	XTAL_FREQ <15:0>	DIVIDERP <10:0>	DIVIDERN <10:0>
32768Hz crystal	0	0x0000	0x8000	0x0001	0x029C
38kHz crystal	0	0x0000	0x9470	0x0001	0x0240
32.768kHz reference clock	1	0x0000	0x8000	0x0001	0x029C
75kHz reference clock	1	0x0001	0x24F8	0x0002	0x0247
12MHz reference clock	1	0x00B7	0x1B00	0x0177	0x02AC
24MHz reference clock	1	0x016E	0x3600	0x02EE	0x02AC
40MHz reference clock	1	0x0262	0x5A00	0x04E2	0x02AC

3.7. Digital Signal Processing

3.7.1. FM Stereo Decoder

The digitized IF signal is fed to the FM demodulator which demodulates the signal and outputs a digital multiplexed (MPX) signal consisting of L+R audio, L-R audio, 19KHz pilot tone and RDS signal. The left channel signal and the right channel signal can be extracted from the MPX signal by simply adding and subtracting the L+R signal and L-R signal. The spectrum diagram is shown in Figure 2.

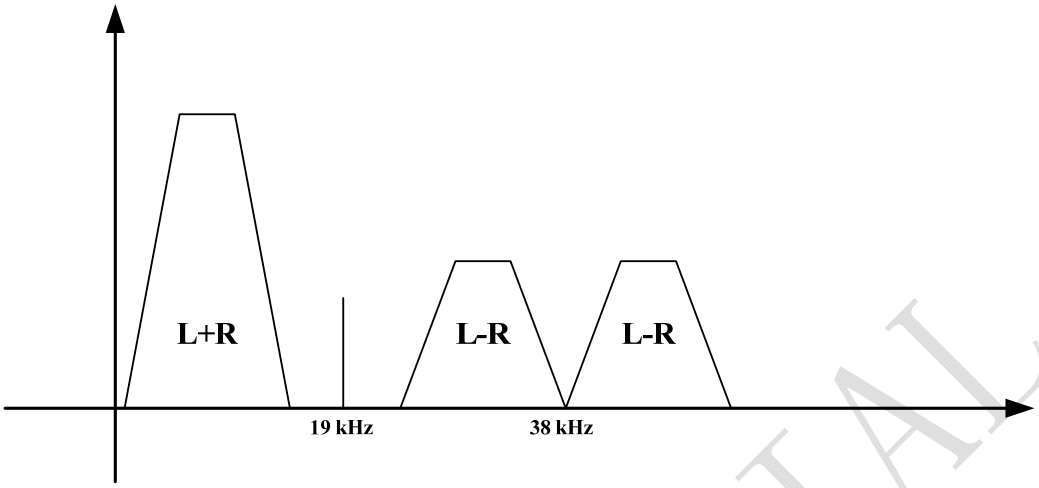


Figure 2: Spectrum diagram of the MPX signal

3.7.2. Mute / Softmute

KT0923 can be hard muted by setting DMUTE to 0 and the output of the audio signal is set to the common mode voltage.

There is also a Soft Mute feature that is enabled by setting FMDSMUTE to 0 in FM mode and AMDSMUTE to 0 in AM mode. In this mode, the audio volume is gradually attenuated when the signal reception is bad (i.e. when the RSSI is below a certain level as defined by FM_SFTMUTE_LOWTH<2:0> and AM_SFTMUTE_LOWTH<2:0>, respectively.) The attenuation attack rate can be configured through SMUTER<1:0>. The target volume can be configured through VOLUMET<2:0>. The volume will be recovery from VOLUMET with a decay rate determined also by SMUTER<1:0> once the signal quality is good enough (i.e. when the RSSI is higher than a certain level as defined by FM_SFTMUTe_HIGHTH<2:0> and AM_SFTMUTE_HIGTH<2:0>, respectively.) SNR value can also be used as the judgment threshold by setting SMMD to 1.

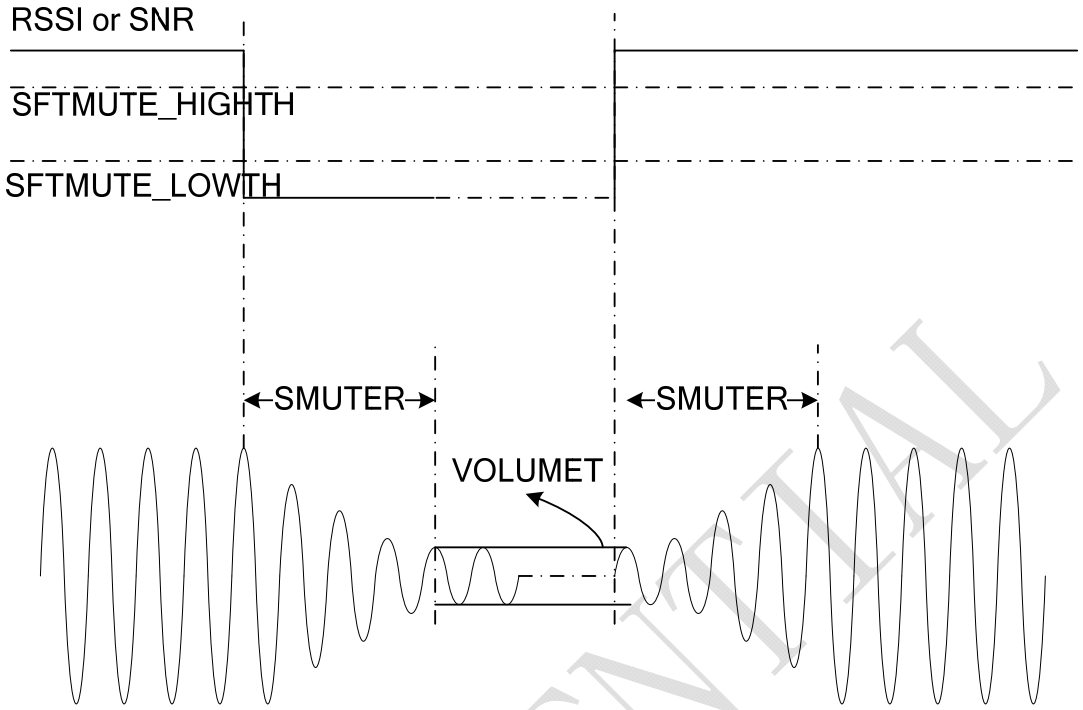


Figure 3 Softmute

3.7.3. Stereo / Mono Blending

In order to provide a comfortable listening experience, KT0923 blends the stereo signal with mono signal gradually when in weak reception in FM mode. The signal level range over which the blending occurs is set by BLNDADJ<1:0>. The blending is disabled when DBLND is set to 1.
MONO playback mode can be forced by setting the MONO to 1.
If the MONO bit and the INV_LEFT_AUDIO bit are both set to 1, then a fully differential signal will be output at the LOUT and ROUT.

3.7.4. Bass

KT0923 provides bass boost feature for audio enhancement. The gain of the bass boost can be programmed through BASS<1:0>. With BASS<1:0>=00, this feature is disabled.

3.7.5. Stereo DAC, Audio Filter and Driver

Two high-quality single-bit ΔΣ audio digital-to-analog converters (DAC) are integrated along with high-fidelity analog audio filters and class AB drivers. Headphones with

impedance as low as 16ohms can be directly driven without adding external audio drivers. An integrated anti-pop circuit suppresses the click-and-pop sound during power up and power down. For different load capacitor, user can set different anti-pop configuration through POP<1:0>.

In order to suit different applications, the gain of the audio driver can be adjusted through register bits AUDV_GAIN<1:0> and to avoid the saturation in output stage, the common mode voltage can also be adjust according to different power supply voltage through register bits AUDV_DCLVL<2:0>.

3.7.6. Line input and TPDT switch

KT0923 integrated three line input drivers and a Three-Poles-Double-Throw switch. User can switch between these three drivers through LINESEL<1:0> bits. By properly set the gain of the line-in drivers through LINEIN_GAIN<2:0>, KT0923 can endure maximum 3Vpp signal with THD less than 0.1%.

3.7.7. AM Bandwidth

KT0923 provides programmable AM channel bandwidth from 1kHz to 5kHz through AM_BW<2:0>.

3.7.8. AM Baseband AGC

KT0923 provides flexible AM baseband AGC configuration to meet the requirements of versatile applications.

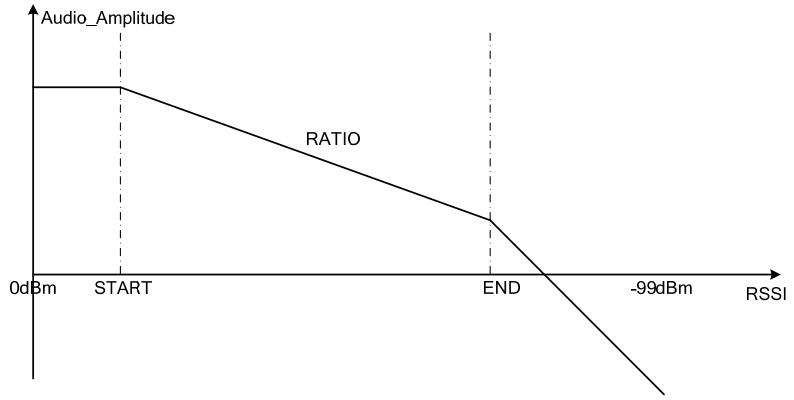


Figure 4 Baseband AGC configuration

Perfect AGC performance (1/inf) is suitable for signal processing but not optimal in RF receiver for the purpose of hearing experience because the volume of the audio signal in AM receiver will be determined directly by the output of the AGC block. In KT0923,

AM_BBAGC_CMP_RATIO<2:0> are used to set different AGC adjusting capability as shown in Figure 4.

There are start point and end point for the compression operation specified by AM_BBAGC_CMP_START<5:0> and AM_BBAGC_CMP_END<5:0>, respectively. Before the start point, AGC has perfect adjusting capability. After that point, the output of AGC will attenuate with the decrease of the input level by the specified compress ratio. Once the input signal strength is less than the compression end point, the output will attenuate with the decrease of input level more drastically avoiding the noise rising effect due to the bad reception condition.

3.7.9. TUNE

The fully integrated LO synthesizer supports wide band operation. Channel tuning is started when the register AMTUNE/FMTUNE is set to 1.

In FM mode, the channel frequency is set by FMCHAN<11:0> and is defined as

$$Freq(KHz) = 50KHz \times FMCHAN<11:0>$$

In AM mode, the channel frequency is set by AMCHAN<14:0> and is defined as

$$Freq(KHz) = 1KHz \times AMCHAN<14:0>$$

3.7.10. SEEK

KT0923 offers effective software based seek algorithm. Refer to application notes for more information.

3.8. I2C Control Interface

The serial interface (I2C mode) is used to read and write the device registers, the external controller can directly read and write a register without going though any other registers first. There is also an internal address counter that automatically moves the pointer forward after a read/write operation so that the external controller can continuously read/write desired number of chip registers starting from any address. The MSB of a register data is transferred first.

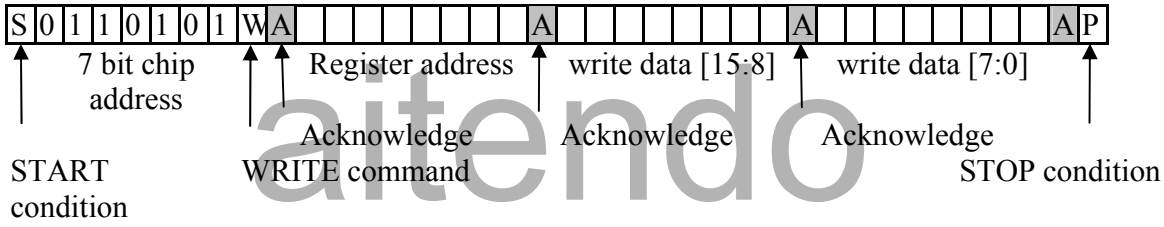
I2C bus mode uses SCL and SDA to transfer data. The device always drives data to SDA at the falling edge of SCL and captures data from SDA at the rising edge of SCL. The device acknowledges the external controller by driving SDA low at the falling edge of SCL. Data transfer always begins with START condition and ends with STOP condition. The external controller can read/write one 16-bits data at the specified address or read/write desired number of registers data continuously from the specified address till STOP condition is occurred.

For write operations, external controller shall send command & data in the following sequence: START condition -> 7 bit chip address and Write command (“0”) -> 8 bit register address n -> write data n [15:8] -> write data n [7:0] -> write data n+1 [15:8] -> write data n+1 [7:0] -> …… -> STOP condition.

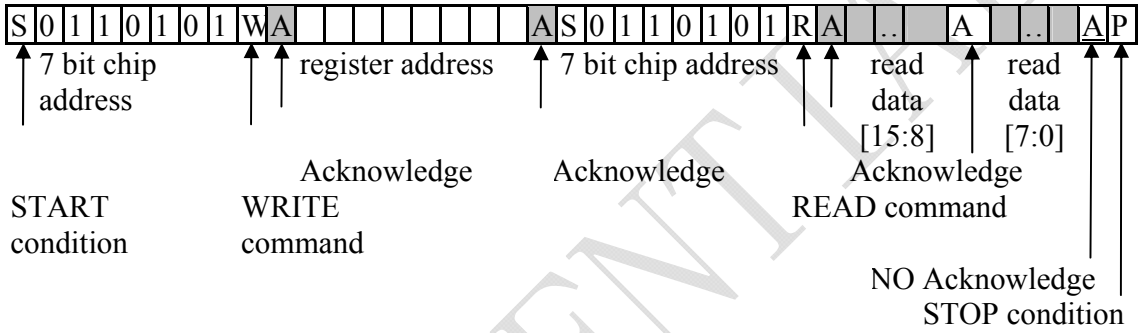
For read operations, external controller shall send command & data in the following sequence: START condition -> 7 bit chip address and Write command (“0”) -> 8 bit register address n -> Repeated-START condition -> 7 bit chip address and Read command (“1”)； then device will send read data n [15:8] -> read data n [7:0] -> read data n+1 [15:8] -> read data n+1 [7:0] -> …… till STOP condition.

Table 7: I2C Interface Protocol

RANDOM REGISTER WRITE PROCEDURE



RANDOM REGISTER READ PROCEDURE



Note: The data bits in gray color are sent by KT0923

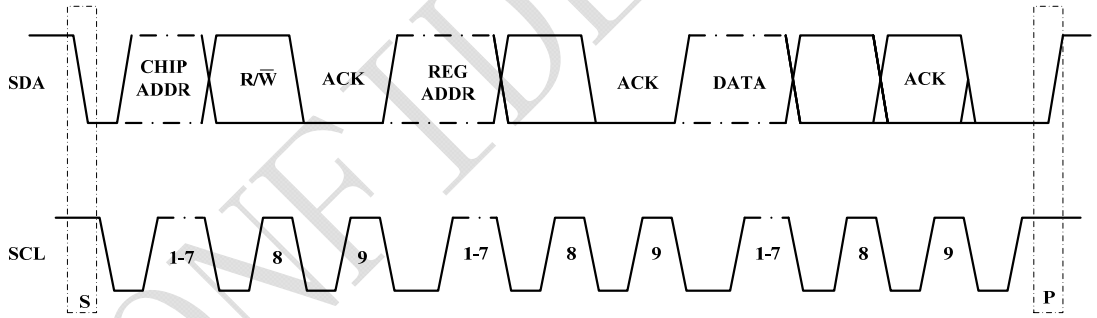
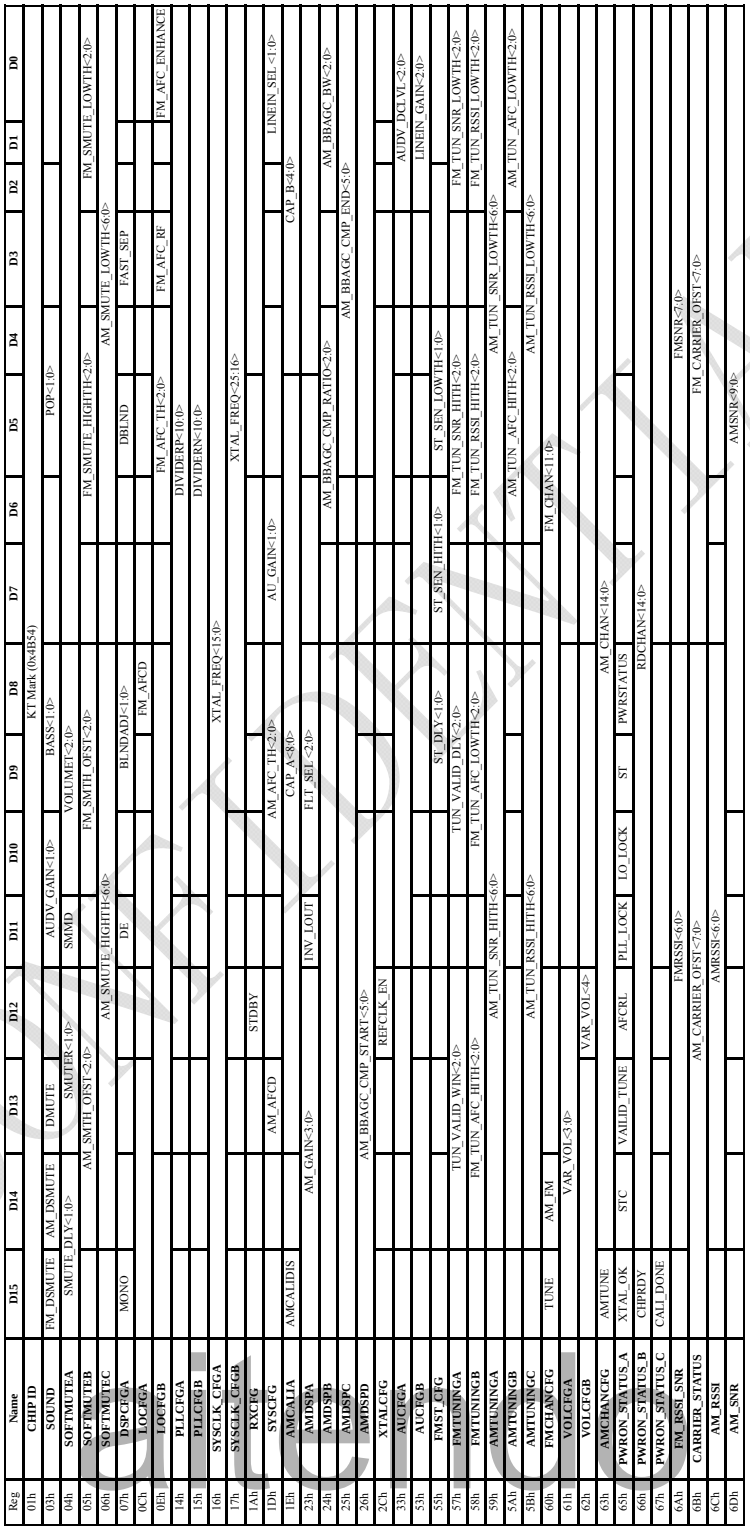


Figure 5: I2C interface timing diagram

3.9. Register Bank



Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
01h	CHIP ID	KT Mark (0x4B54)															
03h	SOUND	FM_DSMUTE	AM_DSMUTE	DMUTE		AUDV_GAIN<1:0>		BASS<1:0>				POP<1:0>					
04h	SOFTMUTEA	SMUTE_DLY<1:0>		SMUTER<1:0>		SMMD		VOLUMET<2:0>									
05h	SOFTMUTEB	AM_SMTH_OFST<2:0>						FM_SMTH_OFST<2:0>				FM_SMUTE_HIGHTH<2:0>				FM_SMUTE_LOWTH<2:0>	
06h	SOFTMUTEC	AM_SMUTE_HIGHTH<6:0>											AM_SMUTE_LOWTH<6:0>				
07h	DSPCFGA	MONO				DE		BLNDADJ<1:0>				DBLND		FAST_SEP			
0Ch	LOCFGA								FM_AFCD					FM_AFC_RF			FM_AFC_ENHANCE
0Eh	LOCFGB											FM_AFC_TH<2:0>					
14h	PLLCFGA											DIVIDERP<10:0>					
15h	PLLCFGB											DIVIDERN<10:0>					
16h	SYSCLK_CFGA																
17h	SYSCLK_CFGB									XTAL_FREQ<15:0>							
1Ah	RXCFG																
1Dh	SYSCFG			AM_AFCD				AM_AFC_TH<2:0>		AU_GAIN<1:0>							
1Eh	AMCALIA	AMCALIDS						CAP_A<8:0>									
23h	AMDSPA																
24h	AMDSPB			AM_GAIN<3:0>		INV_LOUT		FLT_SEL<2:0>				AM_BBAGC_CMP_RATIO<2:0>				AM_BBAGC_BW<2:0>	
25h	AMDSPC																
26h	AMDSPD	AM_BBAGC_CMP_START<5:0>											AM_BBAGC_CMP_END<5:0>				
2Ch	XTALCFG				REFCLK_EN												
33h	AUCFGA															AUDV_DCLVL<2:0>	
53h	AUCFGB															LINEIN_GAIN<2:0>	
55h	FMST_CFG							ST_DLY<1:0>		ST_SEN_HITH<1:0>		ST_SEN_LOWTH<1:0>					
57h	FMTUNINGA	TUN_VALID_WIN<2:0>						TUN_VALID_DLY<2:0>				FM_TUN_SNR_HITH<2:0>				FM_TUN_SNR_LOWTH<2:0>	
58h	FMTUNINGB	FM_TUN_AFC_HITH<2:0>						FM_TUN_AFC_LOWTH<2:0>				FM_TUN_RSSI_HITH<2:0>				FM_TUN_RSSI_LOWTH<2:0>	
59h	AMTUNINGA	AM_TUN_SNR_HITH<6:0>											AM_TUN_SNR_LOWTH<6:0>				
5Ah	AMTUNINGB											AM_TUN_AFC_HITH<2:0>				AM_TUN_AFC_LOWTH<2:0>	
5Bh	AMTUNINGC	AM_TUN_RSSI_HITH<6:0>											AM_TUN_RSSI_LOWTH<6:0>				
60h	FMCHANCFG	TUNE	AM_FM								FM_CHAN<11:0>						
61h	VOLCFGA	VAR_VOL<3:0>															
62h	VOLCFGB				VAR_VOL<4>												
63h	AMCHANCFG	AMTUNE								AM_CHAN<14:0>							
65h	PWRON_STATUS_A	XTAL_OK	STC	VALID_TUNE	AFCRL	PLL_LOCK	LO_LOCK	ST	PWRSTATUS								
66h	PWRON_STATUS_B	CHPRDY							RDCHAN<14:0>								
67h	PWRON_STATUS_C	CALI_DONE															
6Ah	FM_RSSI_SNR	FMRSSI<6:0>											FMSNR<3:0>				
6Bh	CARRIER_STATUS	AM_CARRIER_OFST<7:0>											FM_CARRIER_OFST<7:0>				
6Ch	AM_RSSI	AMRSSI<6:0>															
6Dh	AM_SNR												AMSNR<3:0>				

3.9.1. CHIP ID (Address 0x01)

Bit	Symbol	Access	Default	Functional Description
15:0	KT Mark	R	0x4B54	**ASCII form of string "KT"**

3.9.2. SOUND (Address 0x03)

Bit	Symbol	Access	Default	Functional Description
15	FM_DSMUTE	RW	1	**FM softmute disable**. 0 = enable FM softmute 1 = disable FM softmute
14	AM_DSMUTE	RW	1	**AM softmute disable.** 0 = enable AM softmute 1 = disable AM softmute
13	DMUTE	RW	0	**FM and AM hard mute** 0 = mute disable 1 = mute enable
12	Reserved	RW	0	**Reserved**
11:10	AUDV_GAIN<1:0>	RW	11	**Audio driver gain control** 00 = 0 01 = 2dB 10 = 4dB 11 = 6dB
9:8	BASS<1:0>	RW	00	**Bass boost effect selection** 00 = Disable 01 = Low 10 = Med 11 = High
7:6	Reserved	RW	10	**Reserved**
5:4	POP<1:0>	RW	00	**Audio DAC Anti-pop Configuration** 00 : 100uF AC-coupling capacitor 01 : 60uF AC-coupling capacitor 10 : 20uF AC-coupling capacitor 11 : 10uF AC-coupling capacitor
3:0	Reserved	RW	0100	**Reserved.**

3.9.3. SOFTMUTEA (Address 0x04)

Bit	Symbol	Access	Default	Functional Description
15:14	SMUTE_DLY<1:0>	RW	00	**Delay time after TUNE operation to start softmute operation.** 00 = shortest delay time.

				01 = short delay time. 10 = long delay time. 11 = longest delay time.
13:12	SMUTER<1:0>	RW	00	**Softmute attenuation rate.** 00 = longest softmute time. 01 = long softmute time. 10 = short softmute time. 11 = shortest softmute time.
11	SMMD	RW	0	**Softmute mode selection.** 0 = RSSI mode. 1 = SNR mode.
10:8	VOLUMET<2:0>	RW	000	**Softmute target gain.** 000 = mute 001 = -54dB 010 = -48dB 011 = -40dB 100 = -32dB 101 = -24dB 110 = -16dB 111 = -8dB
7:0	Reserved	RW	0000_0100	**Reserved**

3.9.4. SOFTMUTEB (Address 0x05)

Bit	Symbol	Access	Default	Functional Description
15	Reserved	RW	0	**Reserved.**
14:12	AM_SMTH_OFST<2:0>	RW	000	**Softmute offset value for AM invalid channel; the value set by these bits will be added to AM_SMUTE_HIGHTH and AM_SMUTE_LOWTH respectively when the channel is invalid.** 000 = minimum offset value. …… 111 = maximum offset value.
11	Reserved	RW	0	**Reserved.**
10:8	FM_SMTH_OFST<2:0>	RW	000	**Softmute offset value for FM invalid channel, the value set by these bits will be added to FM_SMUTE_HIGHTH and FM_SMUTE_LOWTH respectively when the channel is invalid.** 000 = minimum offset value.

				…… 111 = maximum offset value.
7	Reserved	RW	0	**Reserved.**
6:4	FM_SMUTE_HIGHTH<2:0>	RW	000	**FM softmute high threshold.** **For RSSI mode:** 000 = minimum RSSI threshold. …… 111 = maximum RSSI threshold. **For SNR mode:** 000 = minimum SNR …… 111 = maximum SNR
3	Reserved	RW	0	
2:0	FM_SMUTE_LOWTH<2:0>	RW	000	**FM softmute low threshold.** **For RSSI mode:** 000 = minimum RSSI threshold. …… 111 = maximum RSSI threshold. **For SNR mode:** 000 = minimum SNR threshold. …… 111 = maximum SNR threshold.

3.9.5. SOFTMUTEC (Address 0x06)

Bit	Symbol	Access	Default	Functional Description
15	Reserved	RW	0	**Reserved.**
14:8	AM_SMTH_HIGHTH<6:0>	RW	000_0000	**AM softmute high threshold.** **For RSSI mode:** 000 = minimum RSSI threshold. …… 111 = maximum RSSI threshold. **For SNR mode:** 0000000 = minimum SNR …… 1111111 = maximum SNR
7	Reserved	RW	0	**Reserved.**
6:0	AM_SMTH_LOWTH<6:0>	RW	000_0000	**AM softmute high threshold.** **For RSSI mode:** 000 = minimum RSSI threshold. …… 111 = maximum RSSI threshold. **For SNR mode:** 0000000 = minimum SNR threshold.

				…… 1111111 = maximum SNR threshold.

3.9.6. DSPCFGA (Address 0x07)

Bit	Symbol	Access	Default	Functional Description
15	MONO	RW	0	**Mono Select** 0 = Stereo mode. 1 = Force to mono mode. **To be noted that if both MONO bit and INV_LOUT are set to 1, fully differential audio signal can be obtained from LOUT and ROUT pin.**
14:12	Reserved	RW	000	**Reserved**
11	DE	RW	0	**De-emphasis Time Constant Selection** 0 = 75us 1 = 50us
10	Reserved	RW	0	**Reserved.**
9:8	BLNDADJ<1:0>	RW	00	**Stereo/Mono Blend Level Adjustment** 00 = High 01 = Highest 10 = Lowest 11 = Low
7:6	Reserved	RW	10	**Reserved**
5	DBLND	RW	0	**Blend Disable** 0 = Blend enable 1 = Blend disable
4	Reserved	RW	0	**Reserved.**
3	FAST_SEP	RW	0	**Fast separation enable** 0 = disable 1 = enable
2:0	Reserved	RW	000	**Reserved**

3.9.7. DSPCFGB (Address 0x09)

Bit	Symbol	Access	Default	Functional Description
15:13	Reserved	RW	001	**Reserved**
12:8	Reserved	RW	0_0000	**Reserved.**
7:3	Reserved	RW	0_0000	**Reserved.**
2:0	FM_AFC_CRC_RANGE <2:0>	RW	001	**FM AFC correction range.** 000 = 100kHz 001 = 125kHz 010 = 150kHz

				011 = 175kHz 100 = 200kHz 101 = 225kHz 110 = 250kHz 111 = 275kHz **NOTE: AFC correction range must be smaller than the LO lock range specified by LO_LOCK_RANGE<2:0>**

3.9.8. RFCFG (Address 0x0B)

Bit	Symbol	Access	Default	Functional Description
15:14	Reserved	RW	0000_0000	**Reserved.**
13:12	IFPGA<1:0>	RW	0000	**IF PGA gain configuration.** 00 = 0dB 01 = 6dB 10 = 9dB 11 = 12dB
11:8	Reserved	RW	0100	**Reserved.**
7:0	Reserved	RW	0000_0000	**Reserved**

3.9.9. LOCFGA (Address 0x0C)

Bit	Symbol	Access	Default	Functional Description
15:13	LO_LOCK_RANGE<2:0>	RW	001	**LO lock range and exceed this range the LO block will be reset and LO_LOCK bit will be set to 0.** **For FM_AFC_ENHANCE = 0** 000 = 12kHz 001 = 14kHz 010 = 20kHz 011 = 25kHz 100 = 2kHz 101 = 4kHz 110 = 8kHz 111 = 10kHz **For FM_AFC_ENHANCE = 1** 000 = 125kHz 001 = 150kHz 010 = 175kHz

				011 = 200kHz 100 = 225kHz 101 = 250kHz 110 = 275kHz 111 = 300kHz
12:9	Reserved	RW	0010	**Reserved.**
8	FM_AFCD	RW	0	**FM AFC disable.** 0 = Enable FM AFC loop. 1 = Disale FM AFC loop.
7:0	Reserved	RW	0010_0000	**Reserved.**

3.9.10. LOCFGB (Address 0x0E)

Bit	Symbol	Access	Default	Functional Description
15:8	Reserved	RW	0000_0000	**Reserved.**
7	Reserved	RW	0	**Reserved.**
6:4	FM_AFC_DET_TH<2:0>	RW	010	**Limiter threshold for FM AFC detection block, if the detected frequency error is larger the specified value, the AFC loop will be stopped and AFCRAIL bit is set to 1.** **For FM_AFC_ENHANCE=0** 000 = 5kHz 001 = 10kHz 010 = 15kHz 011 = 20kHz 100 = 25kHz 101 = 30kHz 110 = 35kHz 111 = 35kHz **For FM_AFC_ENHANCE=1** 000 = 50kHz 001 = 65kHz 010 = 80kHz 011 = 95kHz 100 = 110kHz 101 = 125kHz 110 = 140kHz 111 =155kHz
3	FM_AFC_RF	RW	0	**AFC loop selection** 0 = local AFC loop, i.e., calculate and feedback in DSP block locally. 1 = global AFC loop, i.e., calculate in DSP

				block but feedback to RF block. **NOTE: This bit must be set to 1 if FM AFC enhancement is enabled.**
2:1	Reserved	RW	00	Reserved.
0	FM_AFC_ENHANCE	RW	0	**FM AFC enhancement, used to expand the AFC threshold.** 0 = disable AFC enhancement function. 1 = enable AFC enhancement function. **Note: To enable the AFC_ENHANCE function, FM_AFC_RF bit must be set to 1 and the AFC correction range and LO lock range must be set to proper value.**

3.9.11. PLLCFGA (Address 0x14)

Bit	Symbol	Access	Default	Functional Description
15:11	Reserved	RW	0_0000	**Reserved.**
10:0	DIVIDERP<10:0>	RW	000_0000_0001	PLL divider P configuration

3.9.12. PLLCFGB (Address 0x15)

Bit	Symbol	Access	Default	Functional Description
15:11	Reserved	RW	0_0000	**Reserved.**
10:0	DIVIDERN<10:0>	RW	010_1001_1100	PLL divider N configuration

3.9.13. SYSCLK_CFGA (Address 0x16)

Bit	Symbol	Access	Default	Functional Description
15:0	XTAL_FREQ<15:0>	RW	0x8000	**Lower 16 bits of crystal or reference clock frequency setting.**

3.9.14. SYSCLK_CFGB (Address 0x17)

Bit	Symbol	Access	Default	Functional Description
15:10	Reserved	RW	00_0000	Reserved.
9:0	XTAL_FREQ<25:16>	RW	00_0000_0000	**Higher 10 bits of crystal or reference clock frequency setting.**

3.9.15. SYSCFGA (Address 0x1A)

Bit	Symbol	Access	Default	Functional Description
15:13	Reserved	RW	100	**Reserved.**
12	STDBY	RW	0	**Standby mode control.** 0 = normal operation 1 = standby mode.
11:8	Reserved	RW	0000	
7:0	Reserved	RW	0001_11111	**Reserved.**

3.9.16. SYSCFGB (Address 0x1D)

Bit	Symbol	Access	Default	Functional Description
15	Reserved	RW	0	**Reserved**
14	Reserved	RW	1	Reserved.
13	AM_AFCD	RW	0	**AM AFC disable control.** 0 = AM AFC loop enable. 1 = AM AFC loop disable.
12:11	Reserved	RW	00	**Reserved.**
10:8	AM_AFC_TH<2:0>	RW	010	**AM AFC Threshold.** 000 = 0.5kHz 001 = 1kHz 010 = 2kHz 011 = 3kHz 100 = 6kHz 101 = 10kHz 110 = 12kHz 111 = 15kHz
7:6	AU_GAIN<1:0>	RW	11	**Audio gain for FM audio processor.** 00 = 3dB 01 = 6dB 10 = -3dB 11 = 0dB
5:2	Reserved	RW	0000	**Reserved.**
1:0	LINEIN_SEL<1:0>	RW	00	**Line in path selection.** 00 = all three paths are disable. 01 = Path A is selected. 10 = Path B is selected. 11 = Path C is selected.

3.9.17. AMCALIA (Address 0x1E)

Bit	Symbol	Access	Default	Functional Description
15	AMCALIDIS	RW	0	**AM antenna calibration loop disable.** 0 = enable. 1 = disable.
14	Reserved	RW	0	**Reserved.**
13:5	CAP_A<8:0>	RW	1_1111_1111	**Calibration code A** 0_0000_0000 = none capacitor in group A is selected, for maximum frequency. 1_1111_1111 = all capacitors in group A are selected, for minimum frequency.
4:0	CAP_B<4:0>	RW	0_1111	**Calibration code B** 0_0000 = non capacitor in group B is selected, for maximum frequency. 1_1111 = all capacitors in group B are selected, for minimum frequency.

3.9.18. AMDSPA (Address 0x23)

Bit	Symbol	Access	Default	Functional Description
15:12	AM_GAIN<3:0>	RW	0100	**Audio gain for AM audio processor.** 0000 = 6dB 0001 = 3dB 0010 = 0dB 0011 = -3dB 0100 = -6dB 0101 = -9dB 0110 = -12dB 0111 = -15dB 1000 = -18dB
11	DIFF_LOUT	RW	0	**Differential output enable** 0 = normal operation 1 = output a differential in LOUT and ROUT pins. **NOTE: MONO bit must set to 1 before this bit is set to 1.**
10:8	FLT_SEL<2:0>	RW	001	**AM channel filter bandwidth selection.** 000 = 1kHz 001 = 2kHz 010 = 3kHz 011 = 4kHz

				100 = 5kHz Other = reserved.
7:5	Reserved	RW	000	**Reserved.**
4:0	Reserved	RW	0_0000	**Reserved.**

3.9.19. AMDSPB (Address 0x24)

Bit	Symbol	Access	Default	Functional Description
15:8	Reserved	RW	0000_0100	**Reserved**
7	Reserved	RW	1	**Reserved**
6:4	AM_BBAGC_CMP_RATIO<2:0>	RW	100	**Baseband AGC compression ratio** 000 = 1/inf 001 = 1/16 010 = 1/8 011 = 1/4 100 = 1/3 101 = 1/2 Others = reserved.
3	Reserved	RW	0	**Reserved.**
2:0	AM_BBAGC_BW<2:0>	RW	011	**Baseband AGC bandwidth** 000 = narrowest bandwidth. …… 111 = widest bandwidth.

3.9.20. AMDSPD (Address 0x25)

Bit	Symbol	Access	Default	Functional Description
15:8	Reserved	RW	0000_0001	**Reserved.**
7:6	Reserved	RW	00	**Reserved.**
5:0	AM_BBAGC_CMP_END<5:0>	RW	01_1110	**AM baseband AGC compression end point.** 000000 = 0dBm 000001 = -3dBm 000010 = -6dBm …… 100000 = -96dBm 100001 = -99dBm

3.9.21. AMDSPD (Address 0x26)

Bit	Symbol	Access	Default	Functional Description

15:10	AM_BBAGC_CMP_START<5:0>	RW	01_1110	**AM baseband AGC compression start point.** 000000 = 0dBm 000001 = -3dBm 000010 = -6dBm …… 100000 = -96dBm 100001 = -99dBm
9:8	Reserved	RW	00	**Reserved.**
7:0	Reserved	RW	0000_1000	**Reserved.**

3.9.22. XTALCFG (Address 0x2C)

Bit	Symbol	Access	Default	Functional Description
15:13	Reserved	RW	110	**Reserved.**
12	REFCLK_EN	RW	0	**Reference clock enable.** 0 = crystal 1 = external reference clock.
11:8	Reserved	RW	1100	**Reserved.**
7:0	Reserved	RW	0000_0000	**Reserved.**

3.9.23. AUCFGA (Address 0x33)

Bit	Symbol	Access	Default	Functional Description
15:8	Reserved	RW	0000_0000	**Reserved.**
7:3	Reserved	RW	0_0000	**Reserved.**
2:0	AUDV_DCLVL<2:0>	RW	000	**Common mode voltage setting of audio drive stage.** 000 = 0.85V 001 = 0.95V 010 = 1.05V 011 = 1.15V 100 = 1.2V 101 = 1.35V 110 = 1.5V 111 = 1.6V

3.9.24. AUCFGB (Address 0x53)

Bit	Symbol	Access	Default	Functional Description
15:8	Reserved	RW	0000_0000	**Reserved.**
7:3	Reserved	RW	0_0000	**Reserved.**

2:0	LINEIN_GAIN<2:0>	RW	100	**Gain of the line in stage.** 000 = -12dB 001 = -9dB 010 = -6dB 011 = -3dB 100 = 0dB 101 = 3dB 110 = 6dB 111 = 9dB

3.9.25. FMST_CFG (Address 0x55)

Bit	Symbol	Access	Default	Functional Description
15:10	Reserved	RW	00_0000	**Reserved.**
9:8	ST_DLY<1:0>	RW	00	**Time interval for ST judgement after TUNE operation.** 00 = shortest delay time. …… 11 = longest delay time.
7:6	ST_SEN_HITH<1:0>	RW	00	**Stereo separation sensitivity high threshold.** 00 = -102dBm 01 = -99dBm 10 = -96dBm 11 = -93dBm
5:4	ST_SEN_LOWTH<1:0>	RW	00	**Stereo separation sensitivity low threshold.** 00 = -105dBm 01 = -102dBm 10 = -99dBm 11 = -96dBm
3:0	Reserved	RW	00	**Reserved.**

3.9.26. FMTUNINGA (Address 0x57)

Bit	Symbol	Access	Default	Functional Description
15	Reserved	RW	0	**Reserved.**
14:12	TUNE_VALID_WIN<2:0>	RW	000	**Time interval for valid tuning indicator judgment.** 000 = shortest window time. ….. 111 = longest window time.
11	Reserved	RW	0	**Reserved.**

10:8	TUNE_VALID_DLY<2:0>	RW	000	**First time judgment after TUNE operation.** 000 = shortest delay time. ….. 111 = longest delay time.
7	Reserved	RW	0	**Reserved.**
6:4	FM_TUNE_SNR_HITH<2:0>	RW	000	**SNR high threshold for FM valid channel indicator.** 000 = Minimum SNR threshold. …… 111 = Maxmum SNR threshold.
3	Reserved	RW	0	**Reserved.**
2:0	FM_TUNE_SNR_LOWTH<2:0>	RW	000	**SNR low threshold for FM valid channel indicator.** 000 = Minimum SNR threshold. …… 111 = Maxmum SNR threshold.

3.9.27. FMTUNINGB (Address 0x58)

Bit	Symbol	Access	Default	Functional Description
15	Reserved	RW	0	**Reserved.**
14:12	FM_TUNE_AFC_HITH<2:0>	RW	000	**AFC high threshold for FM valid channel indicator.** 000 = Minimum AFC threshold. …… 111 = Maxmum AFC threshold.
11	Reserved	RW	0	
10:8	FM_TUNE_AFC_LOWTH<2:0>	RW	000	**AFC low threshold for FM valid channel indicator.** 000 = Minimum AFC threshold. …… 111 = Maxmum AFC threshold.
7	Reserved			
6:4	FM_TUNE_RSSI_HITH<2:0>	RW	000	**RSSI high threshold for FM valid channel indicator** 000 = -103dBm 001 = -100dBm 010 = -97dBm 011 = -94dBm 100 = -91dBm 101 = -88dBm 110 = -85dBm 111 = -82dBm

3	Reserved	RW	0	
2:0	FM_TUNE_RSSI_LOWTH<2:0>	RW	000	**RSSI low threshold for FM valid channel indicator** 000 = -106dBm 001 = -103dBm 010 = -100dBm 011 = -97dBm 100 = -94dBm 101 = -91dBm 110 = -88dBm 111 = -85dBm

3.9.28. AMTUNINGA (Address 0x59)

Bit	Symbol	Access	Default	Functional Description
15	Reserved	RW	0	**Reserved.**
14:8	AM_TUNE_SNR_HITH<6:0>	RW	000_0000	**SNR high threshold for AM valid channel indicator** 0000000 = minimum SNR threshold. 1111111 = maximum SNR threshold.
7	Reserved	RW	0	**Reserved.**
6:0	AM_TUNE_SNR_LOWTH<6:0>	RW	000_0000	**SNR low threshold for AM valid channel indicator** 0000000 = minimum SNR threshold. 1111111 = maximum SNR threshold.

3.9.29. AMTUNINGB (Address 0x5A)

Bit	Symbol	Access	Default	Functional Description
15:8	Reserved	RW	0000_000	**Reserved.**
7	Reserved	RW	0	**Reserved.**
6:4	AM_TUNE_AFC_HITH<2:0>	RW	000	**AFC high threshold for AM valid channel indicator** 000 = Minimum AFC threshold. …… 111 = Maxmum AFC threshold.
7	Reserved	RW	0	**Reserved.**
6:0	AM_TUNE_AFC_LOWTH<2:0>	RW	000	**AFC low threshold for AM valid channel indicator** 000 = Minimum AFC threshold. …… 111 = Maxmum AFC threshold.

3.9.30. AMTUNINGC (Address 0x5B)

Bit	Symbol	Access	Default	Functional Description
15	Reserved	RW	0	**Reserved.**
14:8	AM_TUNE_RSSI_HITH<6:0>	RW	000_0000	**RSSI high threshold for AM valid channel indicator** 0000000 = minimum RSSI threshold. 1111111 = maximum RSSI threshold.
7	Reserved	RW	0	**Reserved.**
6:0	AM_TUNE_RSSI_LOWTH<2:0>	RW	000_0000	**RSSI low threshold for AM valid channel indicator** 0000000 = minimum RSSI threshold. 1111111 = maximum RSSI threshold.

3.9.31. FMCHANCFG (Address 0x60)

Bit	Symbol	Access	Default	Functional Description
15	TUNE	RW	0	**FM Tune enable.**
14	AM_FM	RW	0	**AM/FM mode switching** 0 = FM mode. 1 = AM mode.
13:12	Reserved	RW	00	**Reserved.**
11:0	FMCHAN<11:0>	RW	0110_1011_1000	**FM channel with 50kHz step.** Frequency(KHz)=FMCHAN<11:0>*50 kHz

3.9.32. VOLCFGA (Address 0x61)

Bit	Symbol	Access	Default	Functional Description
15:12	VOLUME<3:0>	RW	1111	**Volume configuration**
11:0	Reserved	RW	0000_0000_0000	**Reserved.**

3.9.33. VOLCFGB (Address 0x62)

Bit	Symbol	Access	Default	Functional Description
15:13	Reserved	RW	000	**Reserved**
12	VLUME<4>	RW	1	**Volume control bits together with VOLUME<3:0>:** 11111 = 0dB 11110 = -2dB 11101 = -4dB

				….. 00010 = -58dB 00001 = -60dB 00000 = Mute
11:0	Reserved	RW	0000_0000_0000	**Reserved.**

3.9.34. AMCHANCFG (Address 0x63)

Bit	Symbol	Access	Default	Functional Description
15	AMTUNE	RW	0	**AM Tune enable.**
14:0	AMCHAN<14:0>	RW	000_0001_1111_1000	**AM channel with 1kHz step.**

3.9.35. PWRON_STATUS_A (Address 0x65)

Bit	Symbol	Access	Default	Functional Description
15	XTAL_OK	R	NA	**Crystal ready indictor** 0 = Not ready 1 = Crystal is ok
14	STC	RW	NA	**Seek/Tune Complete** 0 = Not Complete 1 = Complete **Every time the Seek/tune process begins, the STC bit will clear to zero automatically.**
13	VALID_TUNE	R	NA	**Valid channel indicator** 0 = invalid channel. 1 = valid channel.
12	AFCRAIL	R	NA	**AFC rail.** 0 = AFC not railed. 1 = AFC railed.
11	PLL_LOCK	R	NA	**System PLL Ready Indicator** 0 = Not ready 1 = System PLL ready
10	LO_LOCK	R	NA	**LO Synthesizer Ready Indicator** 0 = Not ready 1 = Ready
9	ST	R	NA	**Stereo Indicator** 1 = Stereo state Other = Mono state
8	PWSTATUS	R	NA	**Power on status indicator.** 0 = something wrong in power on sequence. 1 = power on sequence is completed

7:6	Reserved	R	00	**Reserved.**
5	Reserved	R	NA	**Reserved.**
4:0	Reserved	R	0_0000	**Reserved.**

3.9.36. PWRON_STATUS_B (Address 0x66)

Bit	Symbol	Access	Default	Functional Description
15	CHIPRDY	R	NA	**Chip ready indicator.** 0 = chip is not ready for normal operation 1 = chip is ready for normal operation.
14:0	RDCHAN<14:0>	R	NA	**Current Channel Indicator**

3.9.37. PWRON_STATUS_C (Address 0x67)

Bit	Symbol	Access	Default	Functional Description
15	CALI_DONE	R	NA	**Calibration done indicator** 0 = calibration is not finish. 1 = calibration is done.
14:0	Reserved	R	NA	**Reserved**

3.9.38. FM_RSSI_SNR (Address 0x6A)

Bit	Symbol	Access	Default	Functional Description
15	Reserved	R	NA	**Reserved**
14:8	FMRSSI<6:0>	R	NA	**FM rssi value.**
7	Reserved	R	NA	**Reserved.**
6:0	FMSNR<6:0>	R	NA	**FM snr value.**

3.9.39. CARRIER_STATUS (Address 0x6B)

Bit	Symbol	Access	Default	Functional Description
15:8	AM_CARRIER_OFST<7:0>	R	NA	**AM carrier frequency offset**
7:0	FM_CARRIER_OFST<7:0>	R	NA	**FM carrier frequency offset**

3.9.40. AM_RSSI (Address 0x6C)

Bit	Symbol	Access	Default	Functional Description
15	Reserved	R	NA	**Reserved.**
14:8	AMRSSI<6:0>	R	NA	**AM RSSI value.**
7:0	Reserved	R	NA	**Reserved.**

3.9.41. AM_SNR (Address 0x6D)

Bit	Symbol	Access	Default	Functional Description
15:10	Reserved	R	NA	**Reserved.**
9:0	AM_SNR<9:0>	R	NA	**AM SNR value.**

4. Typical Application Circuit

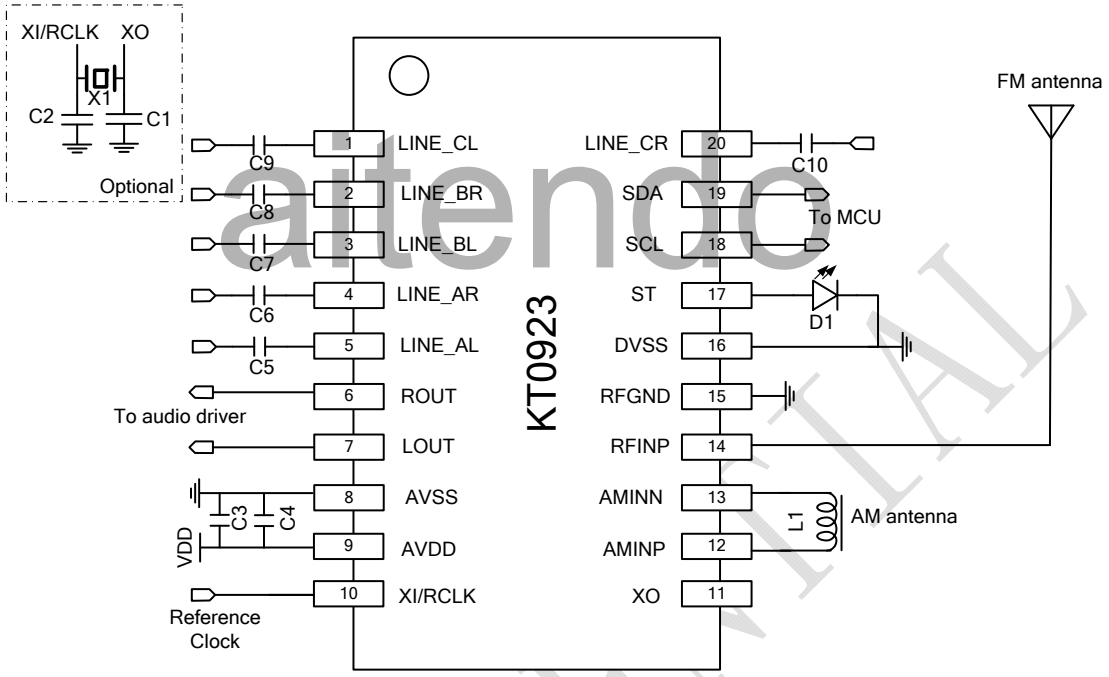
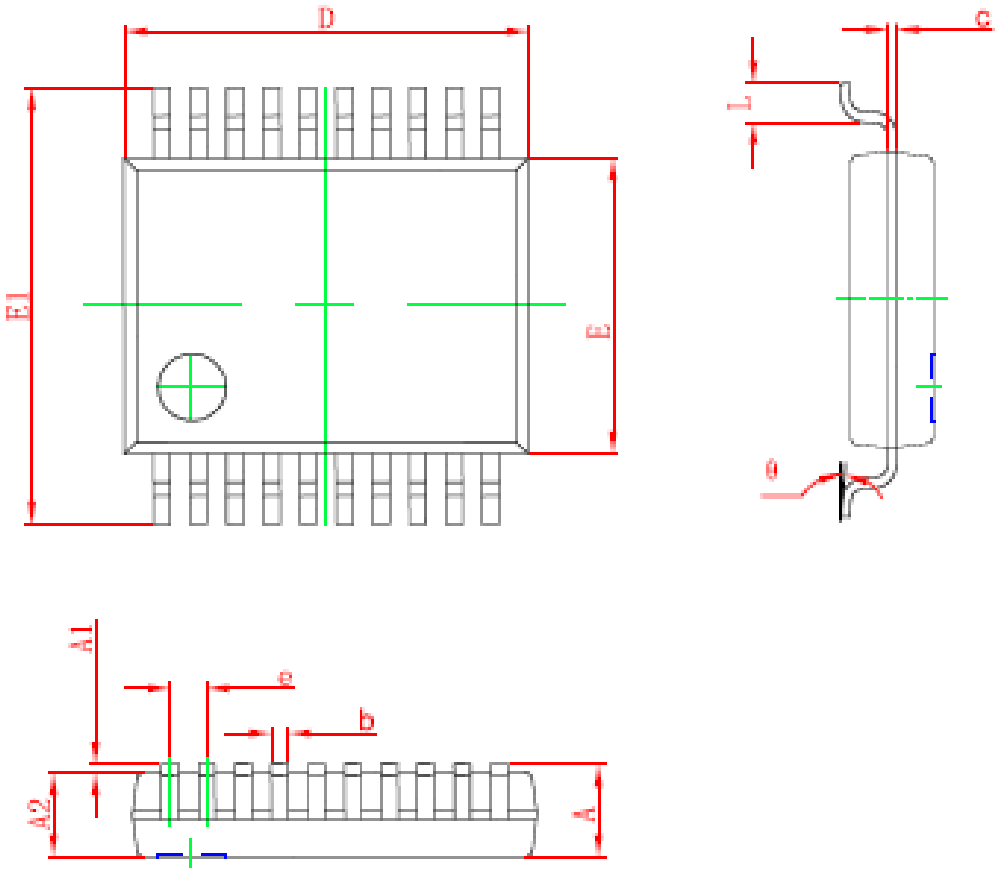


Figure 6: Typical application circuits

Components	Description	Value/Suppliers
C1,C2	Crystal load capacitor	C1=C2=24pF
C3,C4	Supply decoupling capacitor	C3=10uF C4=0.1uF
C5,C6,C7,C8,C9,C10	AC coupling capacitor for line in amplifier	C5~C10=1uF
D1	ST indicator	LED
L1	AM ferrite antenna	300uH
X1	Crystal	32.768KHz or 38kHz

5. Package Outline



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A		1.730		0.068
A1	0.050	0.230	0.002	0.009
A2	1.400	1.600	0.055	0.063
b	0.220	0.380	0.009	0.015
c	0.090	0.250	0.004	0.010
D	7.000	7.400	0.276	0.291
E	5.100	5.500	0.201	0.217
E1	7.600	8.000	0.299	0.315
e	0.65(BSC)		0.026(BSC)	
L	0.550	0.950	0.022	0.037
θ	0°	8°	0°	8°

6. Order Information

Part number	Description	Package	MOQ
KT0923	2nd generation monolithic digital AM/FM receiver	SSOP20L, Pb free	4K pcs

7. Revision History

V1.0 First official release